

Compal Confidential

C5V01 MB Schematic Document

LA-E892P

Rev: 1.A

2017.04.18

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/11/04	Deciphered Date	2018/11/04	Cover Sheet		
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HDMI Conn.

eDP

Interleaved Memory

DDR4-ON BOARD 4G 8Gbx16

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DDI1
HDMI x 4 lanes

eDP

DDI

Memory BUS

Dual Channel

1.2V DDR4 1866/2133

260pin DDR4-SO-DIMM X1

page 20

Nvidia N16S-GTR /
N17S-G1
with GDDR5 x2
page 21~27PCIe 3.0 x 4
8GT/s
port 1-4

page 31

PCIe 3.0 x4
8GT/s
Port 9-12Flexible IO
Base-U PCIe2.0
Premium-U PCIe3.0

Intel Kabylake U

Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)

Processor

Dual Core + GT2
Quad Core + GT2USB 3.0
conn x1
USB3 port 1
USB2 port 1USB 2.0
conn x2
USB2 port3,4
on Sub/BCMOS
Camera
USB2 port 7USB TypeC
conn x1
USB3 port 2,3
USB2 port2

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USBx8 48MHz

HD Audio

3.3V 24MHz

Touch
ScreenUSB2 port 6
page 28HDA Codec
ALC255
page 32

SPI

SPI ROM
64MB
page 9

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022
page 37

Int.KBD



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Touch Pad
PS2 (from EC) / I2C (from SOC)
USB2 port 8 (FP)

page 38

Int. Speaker
page 32Int. DMIC
on Camera
page 28UAI
on Sub/B
page 36

RTC CKT.

page 15

Fan Control

page 39

Power On/Off CKT.

page 38

DC/DC Interface CKT.

page 40

Power Circuit DC/DC

page 41~54

Sub Board

LS-E891
IO/B
page 36LS-E892
Hall Sensor/B
page 38

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Vcc	3.3V +/- 5%					
Ra	100K +/- 1%					
Board ID	Rb	V _{SD} min	V _{SD} typ	V _{SD} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1 (EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	1.0 (DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	1.A (PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1.A (MP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	1.A (EA17PVT)
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	1.A (EA17MP)
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
Acer BYOC	BYOC@ / NBYOC@
CODEC(ALC255)	255@
EC Mode Select	LPC@ / ESPI@
For Intel CMC	CMC@
LAN Mode Select	SWR@ / LDO@
EMI requirement	EMI@ / @EMI@
ESD requirement	ESD@ / @ESD@
RF requirement	@RF@
CPU Selection	U42@/U22@
SkyLake or KabyLake	SKL@ / KBL@
TPM	TPM@
Finger Print	FP@/FPMC@
UMA or DGPU	UMA@/VGA@
DGPU Serial Select	N16X@/N17S@

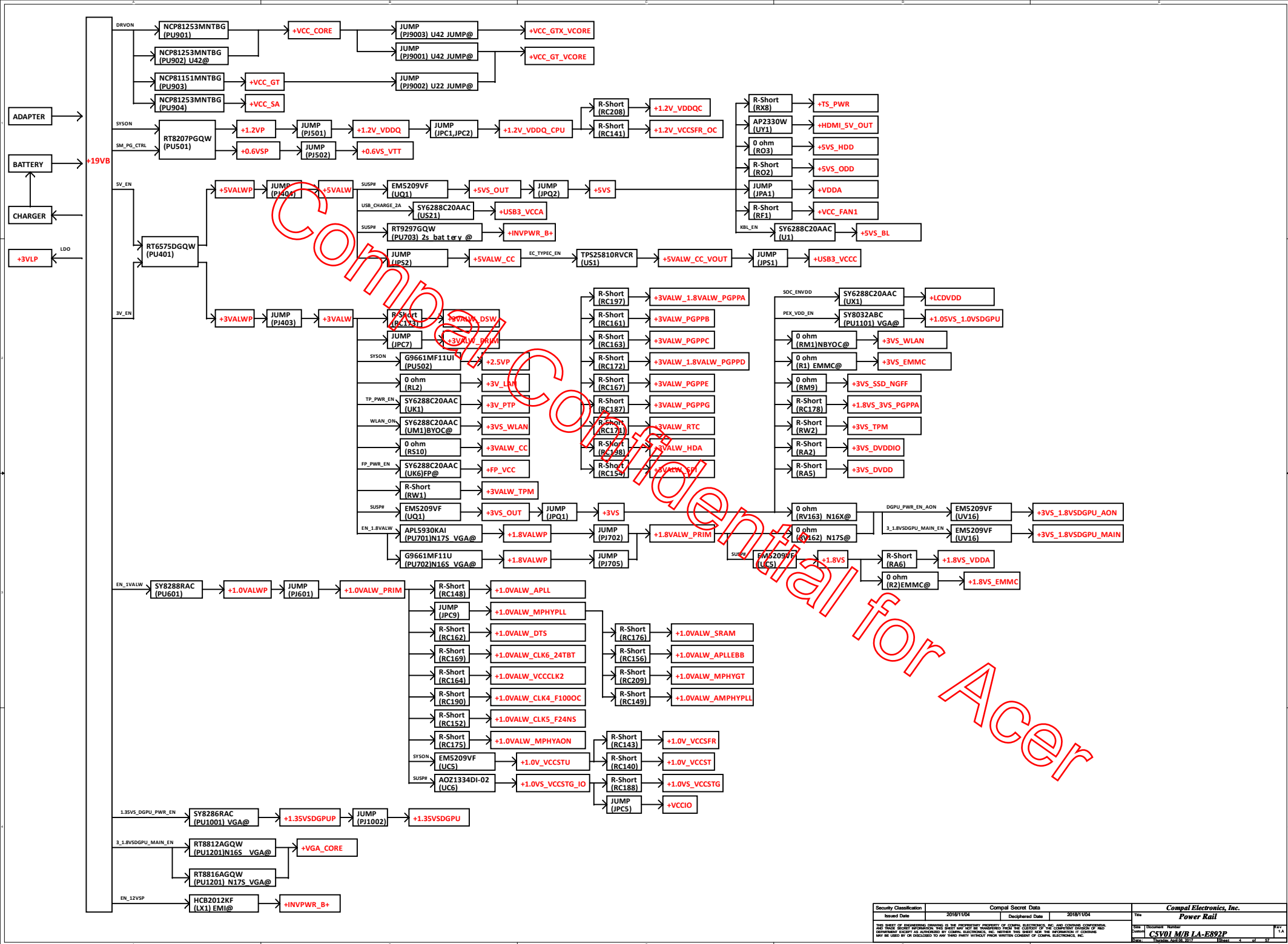
BOM Option Table	
Item	BOM Structure
MB Stage	EM@ / PVT@ / PVT@ / MP@
ODD Support	ODD@
G Sensor	BA@
For over 3 cell battery	3S@
C5V01, D5P1	EA15@
D7W01	EA17@
D7W01 MB Stage	EA17PVT@ / EA17MP@
N16SGTR or N17SG1	N16SGTR@ / N17SG1@
BOM Select	X76@
VRAM BOM Select	X7604@ ~ X7609@
Memory Select	X7601@ ~ X7603@
Memory Mode	SDP@ / DDP@
CPU Code	SR2UW@ QLDP@ / QLDM@ / QLDN@ QLYK@ / QLYJ@ / QLYH@ SR2ZW@ / SR2ZU@ / SR2ZV@ SR343@ / SR342@ / SR341@ QN5D@ / QN5C@

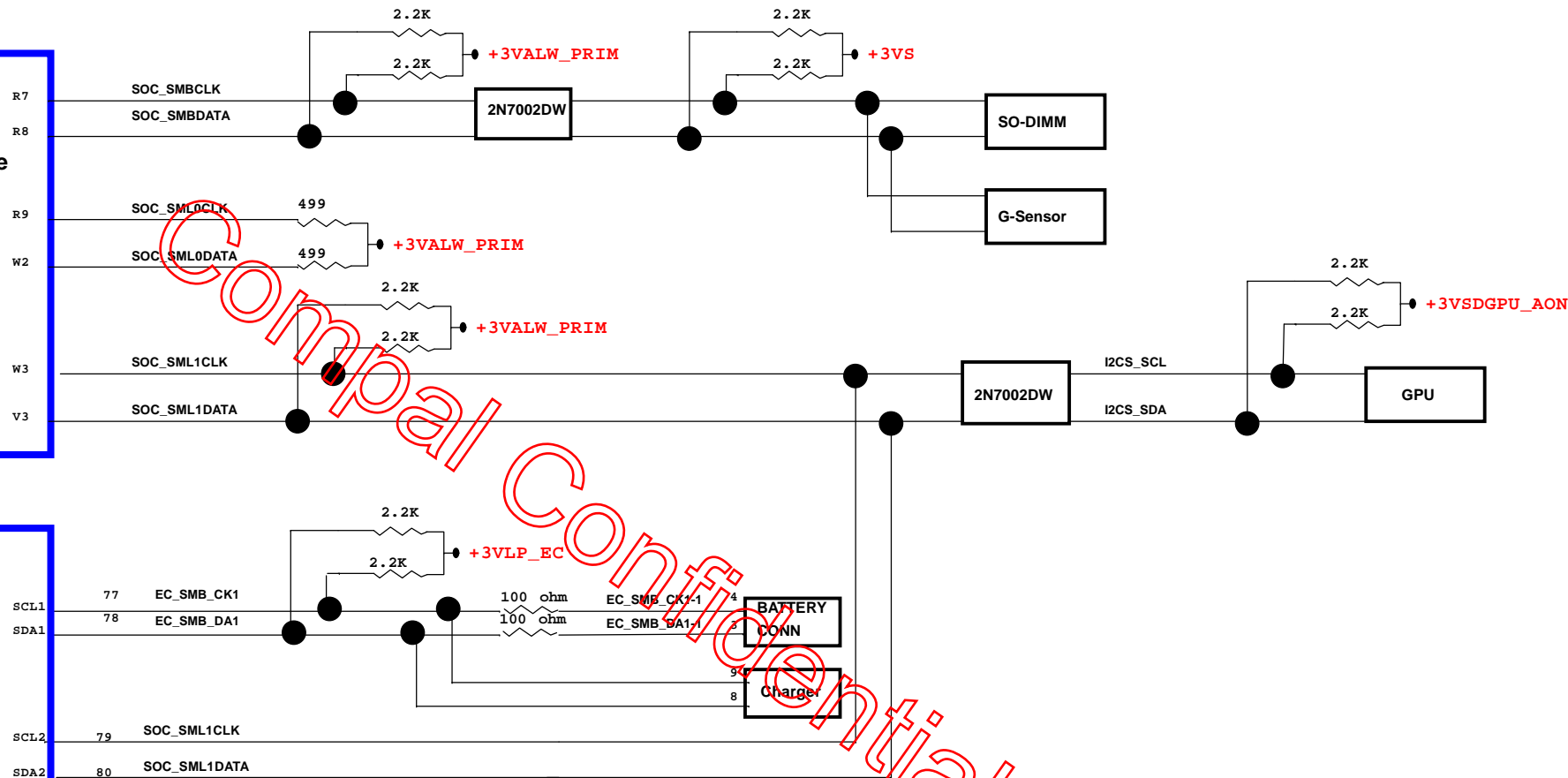
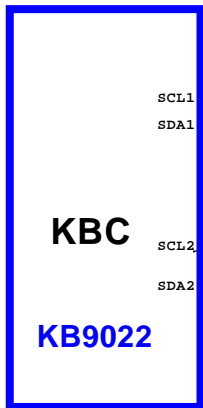
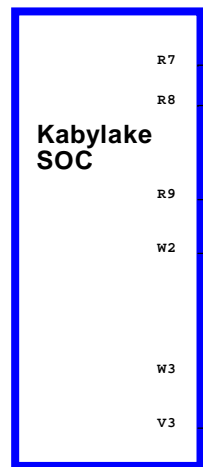
43 Level	Description	BOM Structure
431A7EBOL07	SMT MB AE892 C5V01 N172G I36006 HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR2UW@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL08	SMT MB AE892 C5V01 N172G I57200 1.4HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR2ZU@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL10	SMT MB AE892 C5V01 N172G I77500 1.4HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR2ZV@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL11	SMT MB AE892 C5V01 SGT2G I3-6006U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N16SGTR@/N16X@/NBYOC@/SR2UW@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL15	SMT MB AE892 C5V01 SGT2G I77500 1.4HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N16SGTR@/N16X@/NBYOC@/SR2ZV@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL16	SMT MB AE892 C5V01 SGT2G I3-7100U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N16SGTR@/N16X@/NBYOC@/SR343@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL17	SMT MB AE892 C5V01 SGT2G I5-7200U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N16SGTR@/N16X@/NBYOC@/SR342@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL18	SMT MB AE892 C5V01 SGT2G I7-7500U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N16SGTR@/N16X@/NBYOC@/SR341@/U22@/VGA@/X7601@/X7604@/X4E01@/EA15@
431A7EBOL19	SMT MB AE892 C5V01 N172G I3-7100U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR343@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL20	SMT MB AE892 C5V01 N172G I5-7200U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR342@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@
431A7EBOL21	SMT MB AE892 C5V01 N172G I7-7500U HDMI	255e/3S@/CHG@/CMC@/MP@/KBL@/LD@/LPC@/N17S@/N17SG1@/NBYOC@/SR341@/U22@/VGA@/X7601@/X7607@/X4E02@/EA15@

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVC	RTC Battery Power	ON	ON	ON
+1.05VS_1.0VSDGPU	+1.05VS power rail for N16X/ +1.0VS power rail for N17S	ON*2	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON*2	OFF	OFF
+3VS_1.8VSDGPU_AON	+3VS power rail for N16X/ +1.8VS power rail for N17S(AON)	ON*2	OFF	OFF
+3VS_1.8VSDGPU_MAIN	+3VS power rail for N16X/ +1.8VS power rail for N17S(MAIN)	ON*2	OFF	OFF
+VGA_CORE	Core power for discrete GPU	ON*2	OFF	OFF

Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.
ON*2 power plane is ON when DGPU turn on



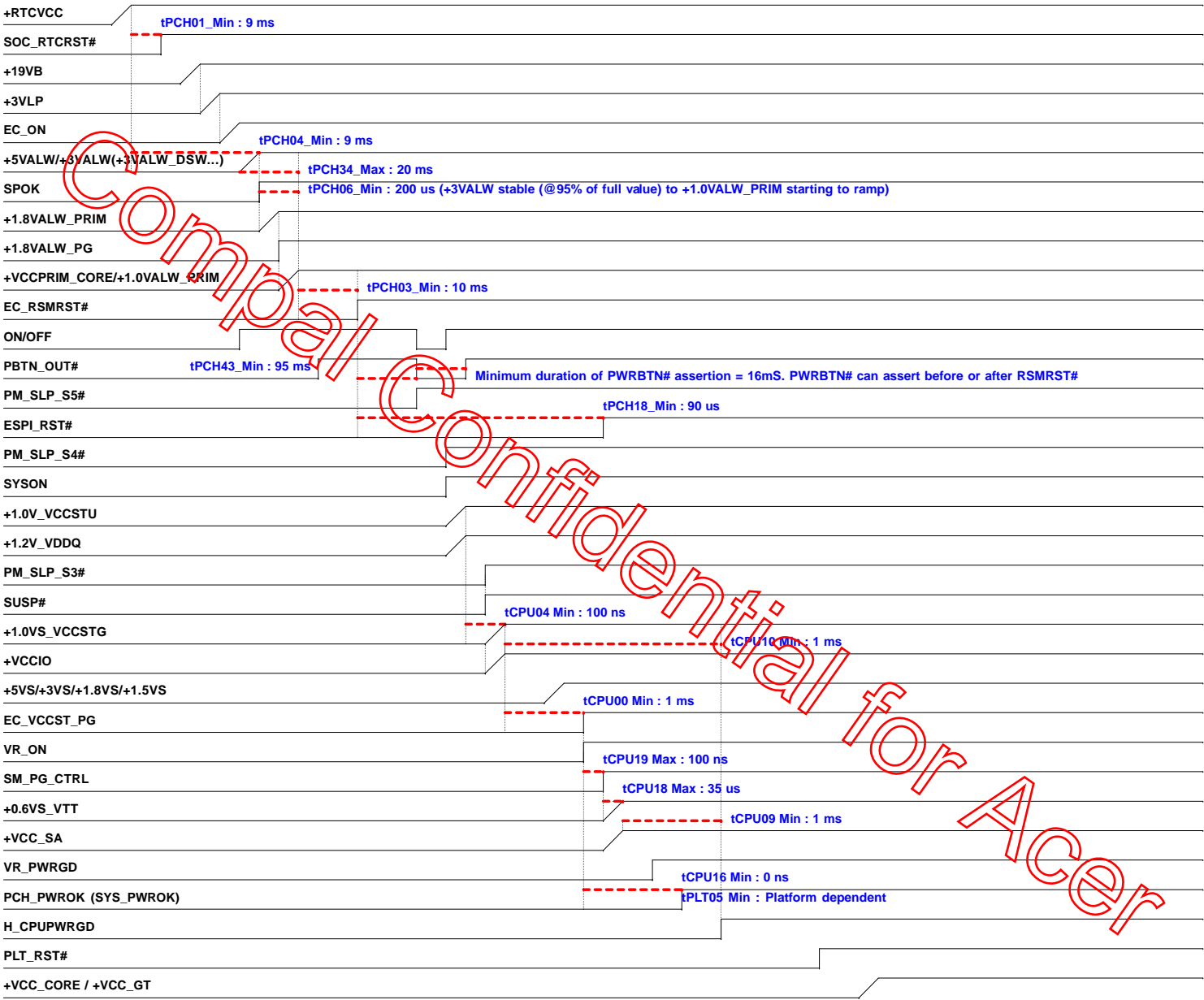


I2C Address Table

Need check

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved			
I2C_1 (+3VALW_PGPPC)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	SO-DIMM	0xA4		
	G-Sensor	0x30		
SOC_SML1CLK +3VALW_PRIM	VGA	0x9E		
	EC			
EC_SMB_CK1 +3VLP	BQ24735 (Charger IC)	0x12		
	BATTERY PACK	0x16		

PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS

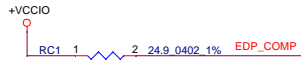


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Size		Document Number		Rev	
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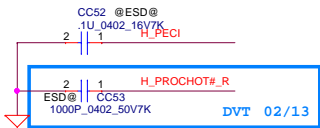
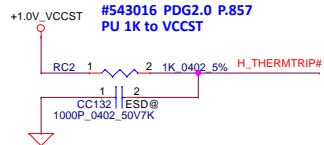
Functional Strap Definitions

#543016 PDG2.0 P.844

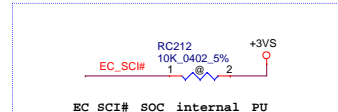
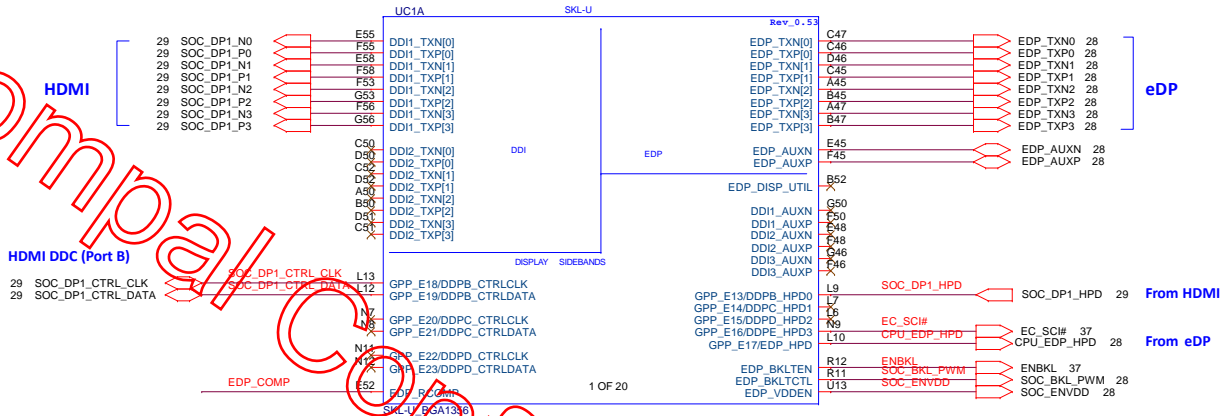
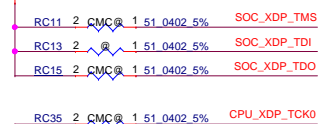
DDPB_CTRLDATA
DDPC_CTRLDATA
Display Port B/C Detected
NC =Port is not detected.
PU =Port is detected.



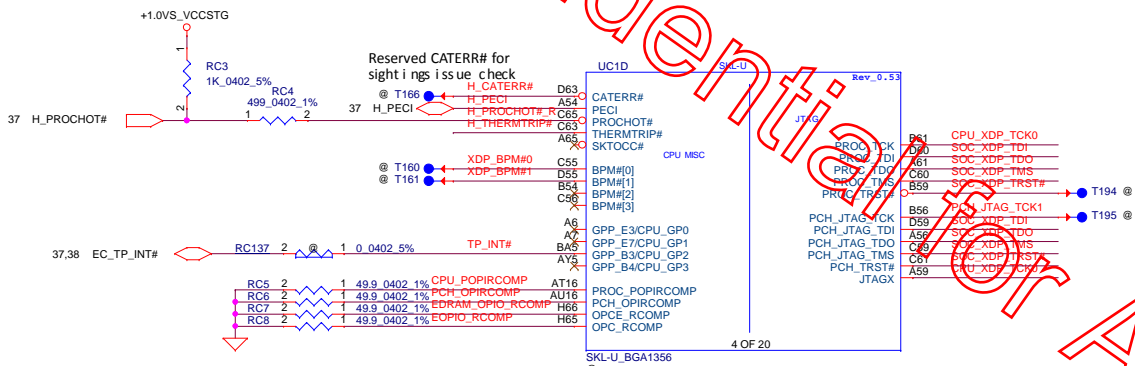
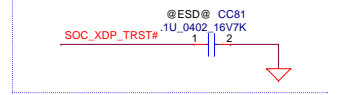
#543016 PDG2.0 P.225
COMPENSATION PU for eDP
Trace width=5 mils,Spacing=25mil,Max length=600mils



+1.0VS_VCCSTG For Intel debug, place to CPU side.
#543016 PDG2.0 P.629



#545659 PCH EDS1.51 P.131
SCI capability is available on all GPIOs, while NMI and SMI capability is available on only select GPIOs.
Below are the PCH GPIOs that can be routed to generate SMI# or NMI:
• GPP_B14 GPP_B20 GPP_B23
• GPP_C[23 : 22]
• GPP_D[4 : 0]
• GPP_E[8 : 0], GPP_E[16 : 13]

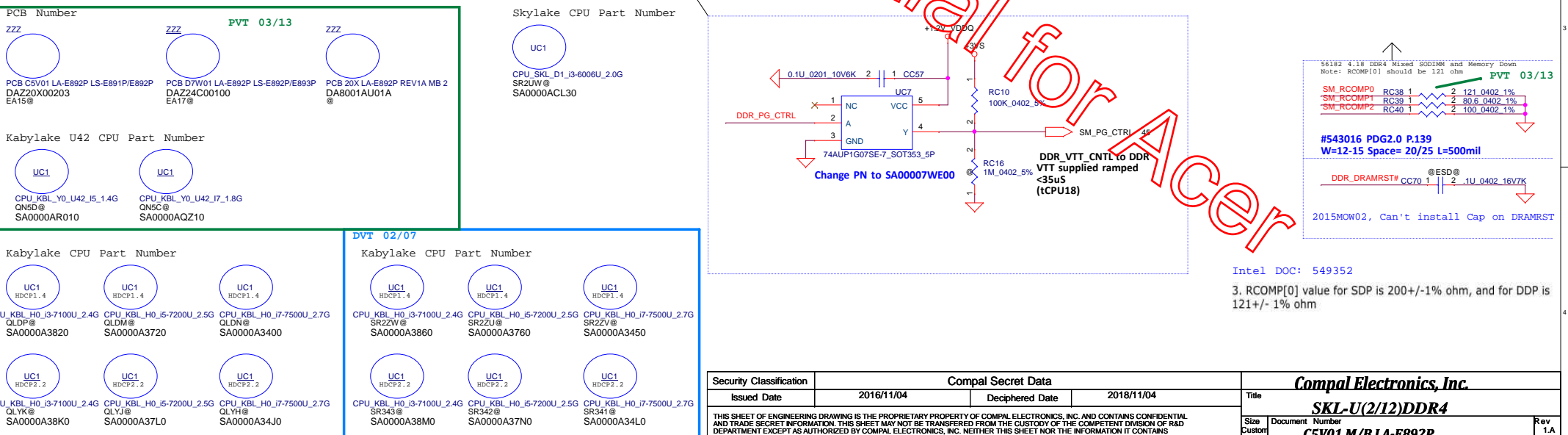
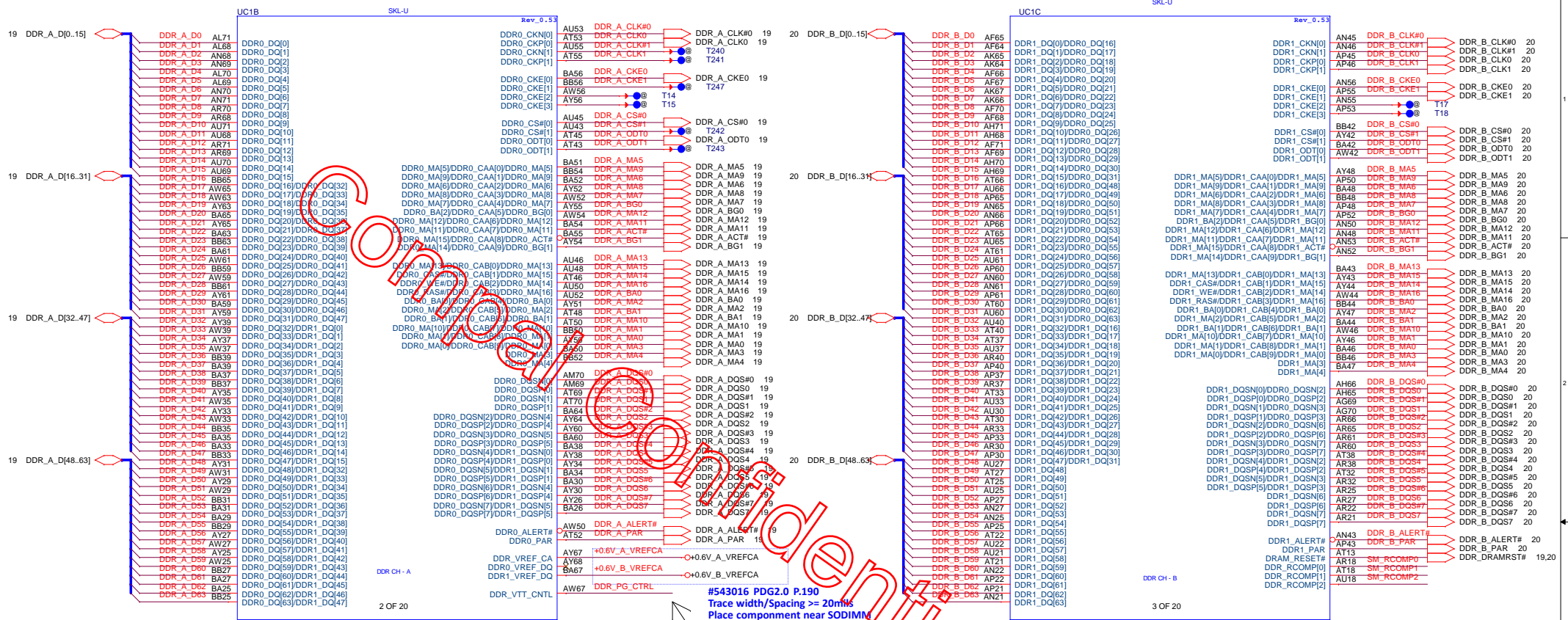


#543016 PDG2.0 P.873
PROC_POPIRCOMP/PCH_OPIRCOMP
PD 50ohm

#544669 CRB1.1 P.52
EDRAM_OPIO_RCOMP/EOPIO_RCOMP
PD 50ohm

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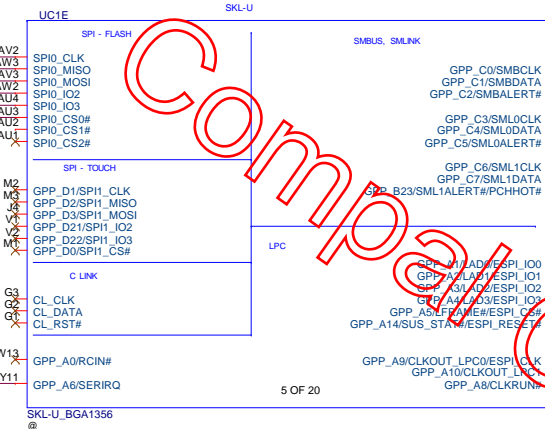
Interleaved Memory



SPI ROM

SOC_SPI_CLK
SOC_SPI_SO
SOC_SPI_SI
SOC_SPI_I02
SOC_SPI_I03
SOC_SPI_CS#0

SPI Touch



SMB (to DDR, G sensor)

SMB (to DDR, G sensor)

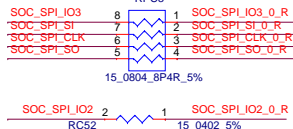
SML1 (to EC, Thermal sensor)

Change RC144-RC147, RC45 to 15ohm when use ESPI

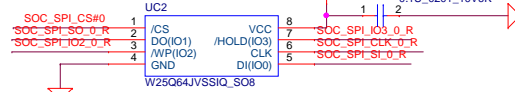
ESPI / LPC Bus
ESPI: +1.8V
*LPC: +3.3V

To EC

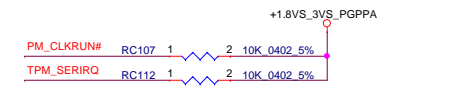
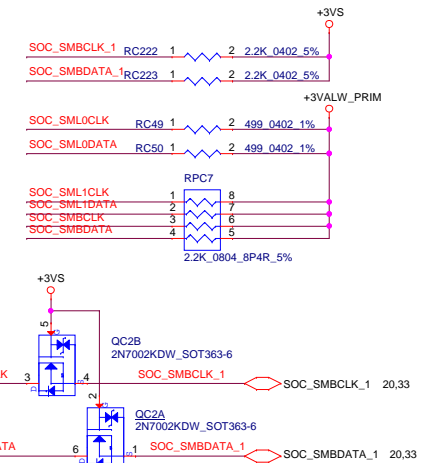
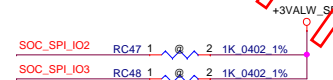
RPCS and RC52 are close UC2



SPI ROM (8MByte)



2015MOW06 no need PU1K on SPI_I02/I03



SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

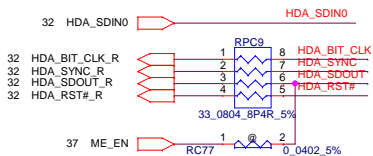
eSPI or LPC
* 0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
* 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto (TLS) (with confidentiality).
Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

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HDA for AUDIO

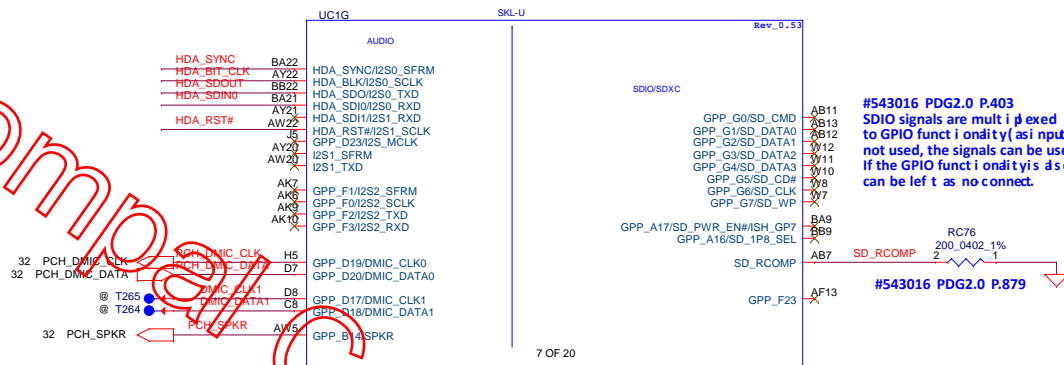


HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)

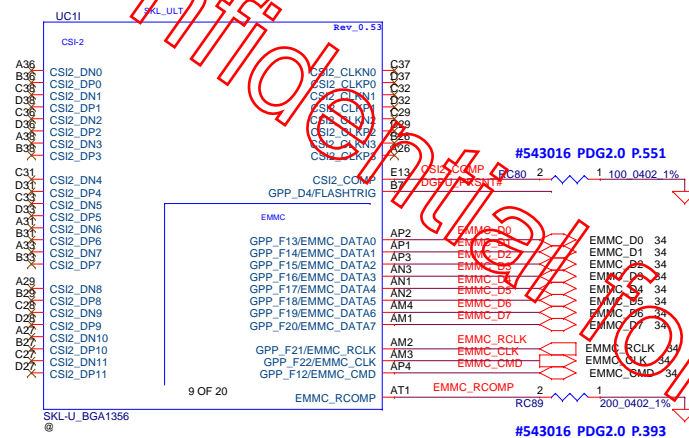
TOP Swap Override
0 = Disable TOP Swap mode.
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable frequency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



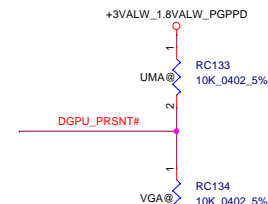
#543016 PDG2.0 P.403
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interfaces not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used the signals can be left as no connect.

#543016 PDG2.0 P.879

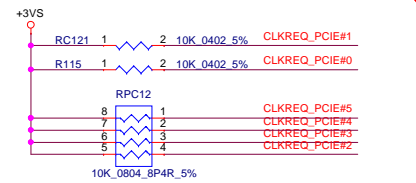
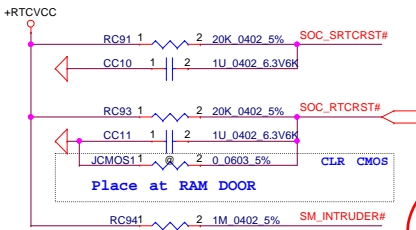


#543016 PDG2.0 P.551

#543016 PDG2.0 P.393

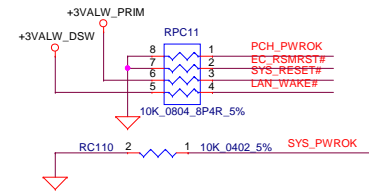


	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

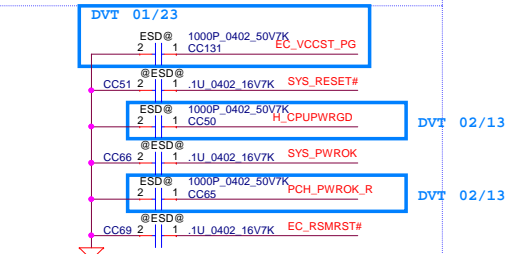


From EC(open-drain)

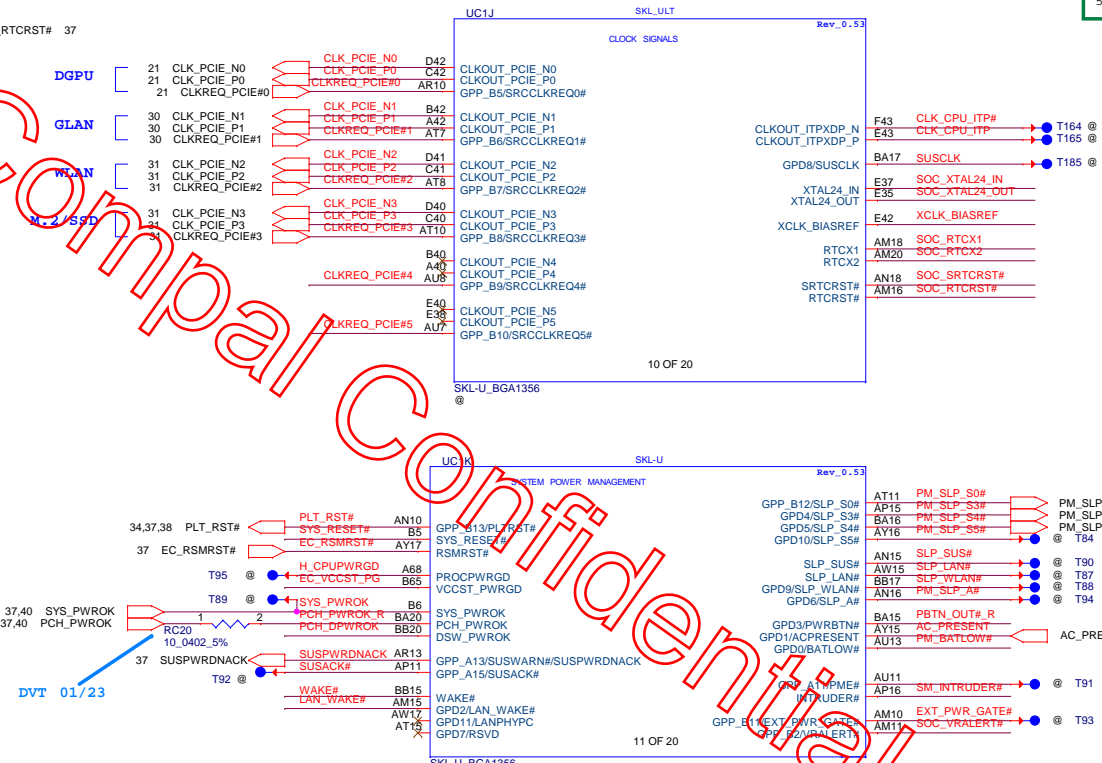
Note for VCCST_PWRGD
 1. 1.0V tolerance
 2. PDG2.0 P.598 Figure43-5 note17: when failure events, VCCST_PWRGD and PCH_PWROK de-assert at the same time



WAKE# (DSX wake event)
 10K pull-up to VccDS W8_3
 The pull-up is required even if PCIe* interface is not used on the platform



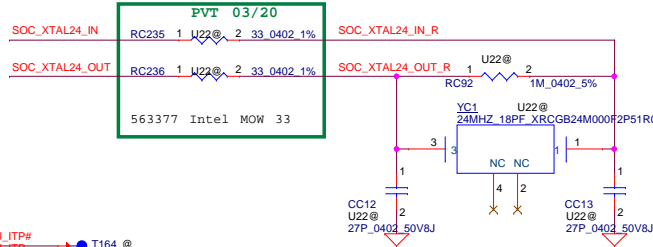
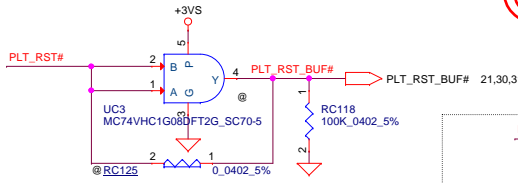
#543016 PDG2.0 P.599
 PROC_PWRGD is used only for power sequence debug and is not required to be connected to anything on the platform



DVT 01/23

Compal Confidential for Acer

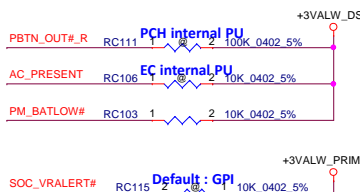
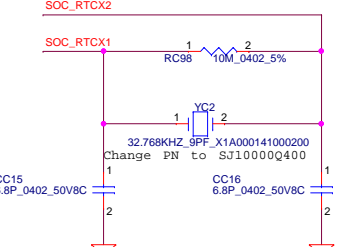
PCH PLTRST Buffer



Follow 2014MOW48
 Skylake U PU 2.7k ohm to 1V
 Cannonlake U PD 60.4 ohm

XCLK_BIASREF
 T:50ohm S:12/15 L:1000 Via:2

2014MOW48:
 Skylake-U use 24M 50 ohm ESR
 Cannonlake U use 38.4M 30 ohm ESR



SOC_VRALERT# Default: GPI

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				SKL-U(5/12)CLK,GPIO	
				Size	
				Custom	
				CSV01 M/B LA-E892P	
				Rev	
				1.A	
				Date: Thursday, April 06, 2017	
				Sheet 11 of 57	

Confidential for Accep

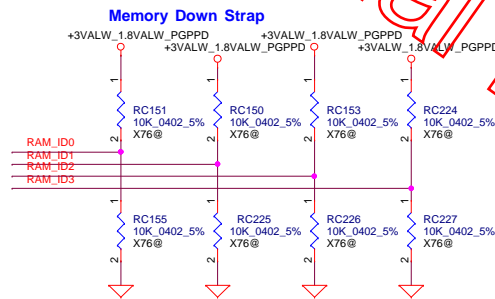
Functional Strap Definitions

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

- *0 = Disable No Reboot Mode. --> AAX05 Use
- 1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

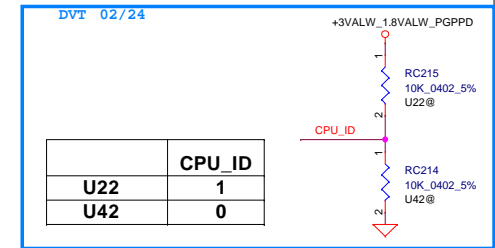
GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

- Boot BIOS Strap Bit
- *0 = SPI Mode --> AAX05 Use
- 1 = LPC Mode

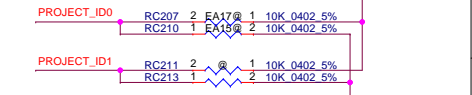


ZZZ	Hynix4GB	X7602@	X76739BOL02
ZZZ	Micron4GB	X7603@	X76739BOL03
ZZZ	Samsung4GB	X7601@	X76739BOL01

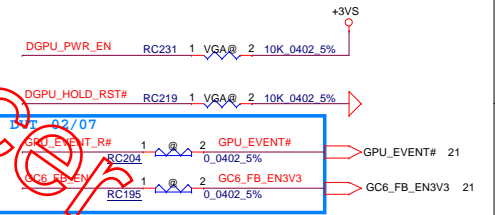
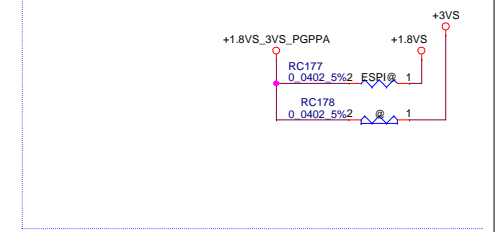
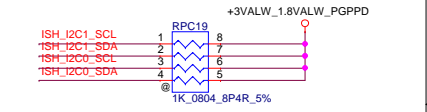
	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4GB	0	0	0	0	SA0000A1H20 (S IC D4 512M16 H5AN8G6NFA-UHC FBGA ABO I)
Micron 4GB	0	0	0	1	SA00009V220 (S IC D4 512M16 MT40A512M16Y-083E:B ABO I)
Samsung 4GB	0	0	1	0	SA00009U420 (S IC D4 512M16 K4A8G16SWB-BCRC FBGA 96P ABO I)
	0	0	1	1	
No OnBoard Memory	1	1	1	1	No On Board Memory



	CPU_ID
U22	1
U42	0



Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* C5V01/D5PR1	0	0
D7W01	0	1
Reserved	1	0
Reserved	1	1



DGPU

GLAN

NGFF WLAN+BT(Key E)

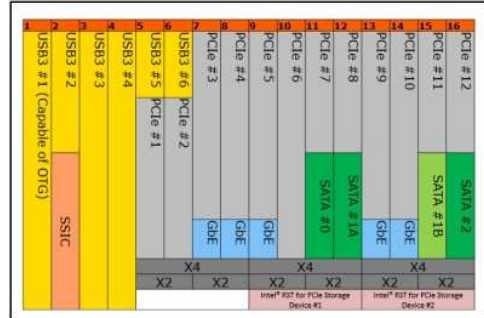
HDD

ODD

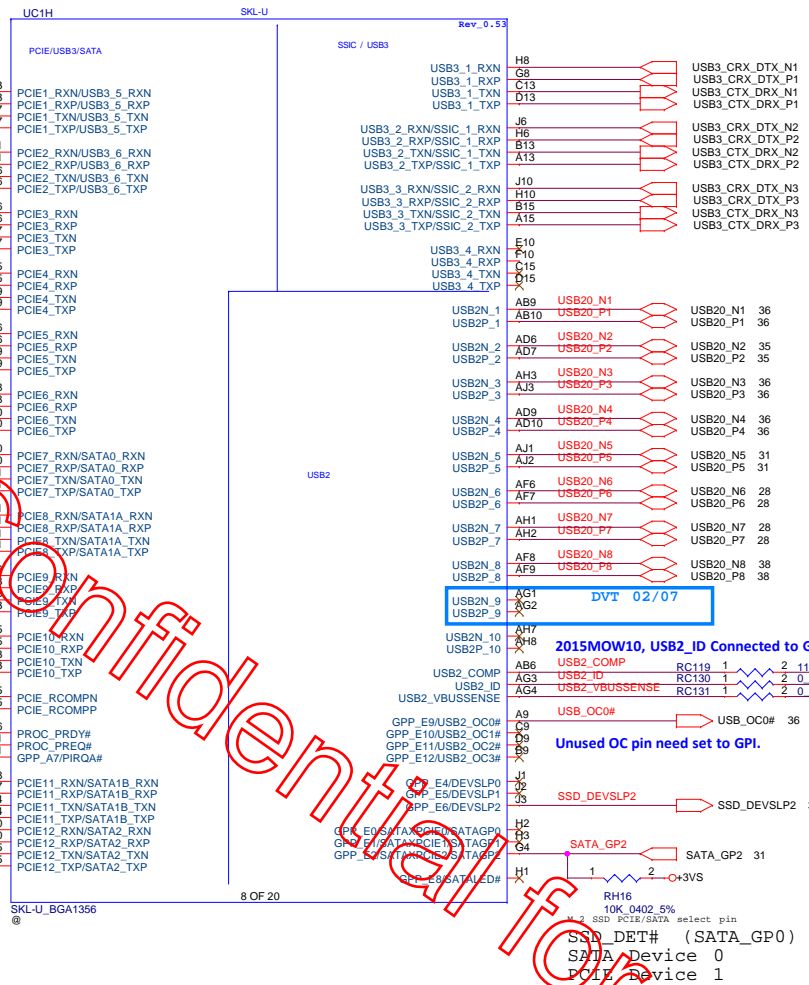
NGFF SSD(Key M)
(Need Lane Reversal)

#543016 PDG2.0 P.285
PCIE_RCOMPEN/PCIE_RCOMPMP
BO=4 W=12 S=12 R=100ohm

HSIO Multiplexing on PCH-U



PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	1x2+2x1	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x1+1x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
Premium-U	1x4	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	1x2+2x1	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x1+1x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23



GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

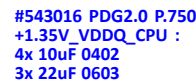
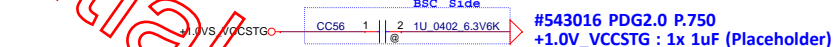
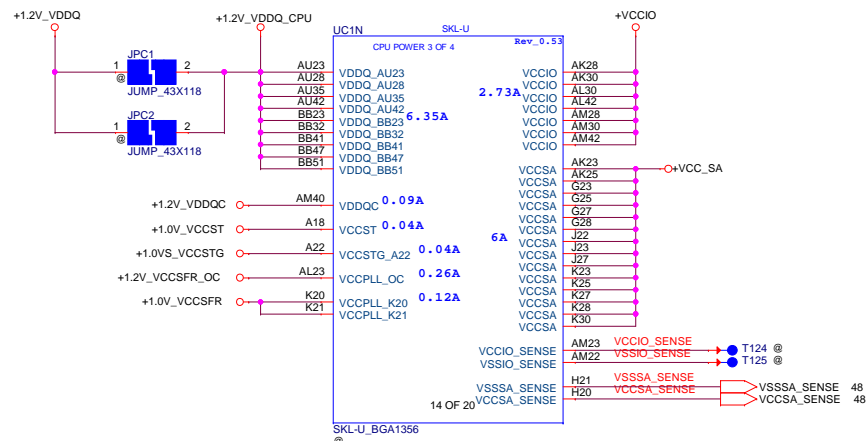
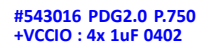
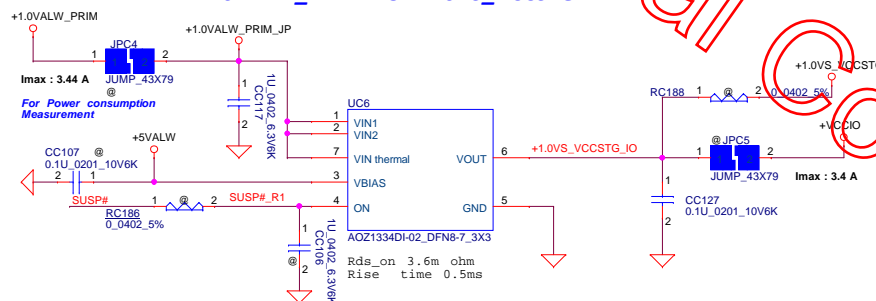
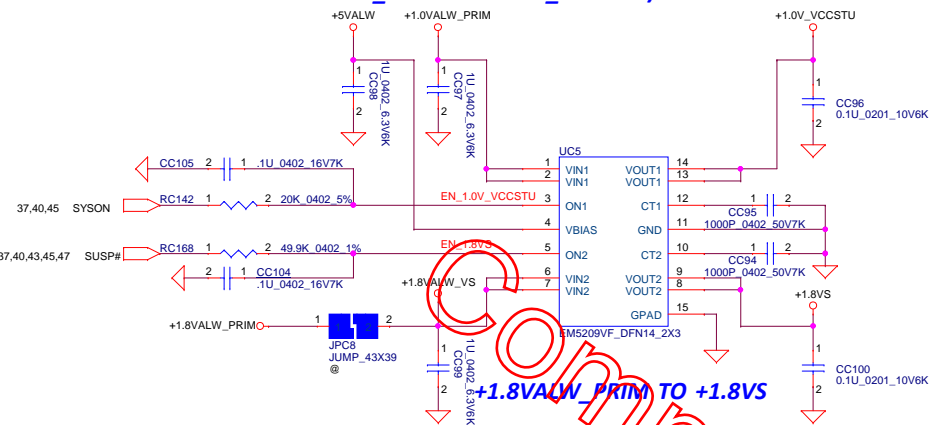
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interconnect power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL-U.

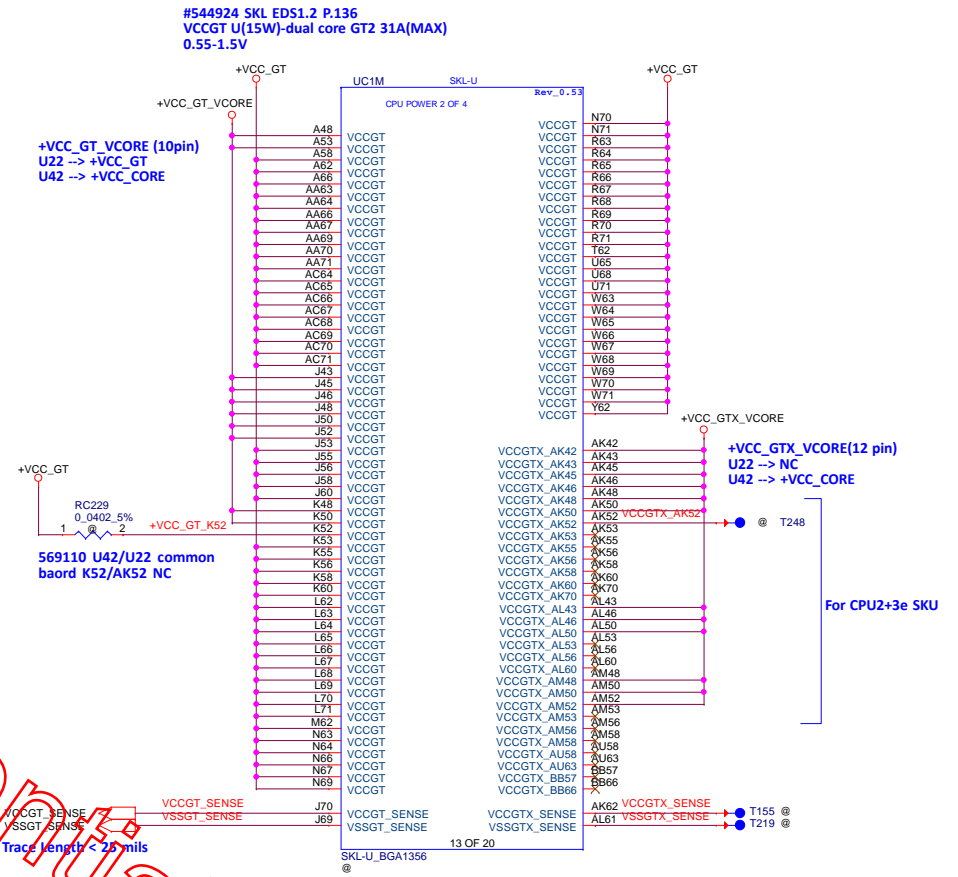
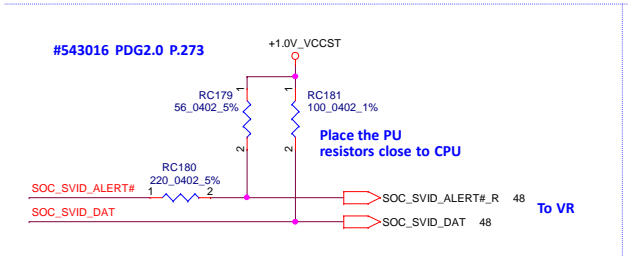
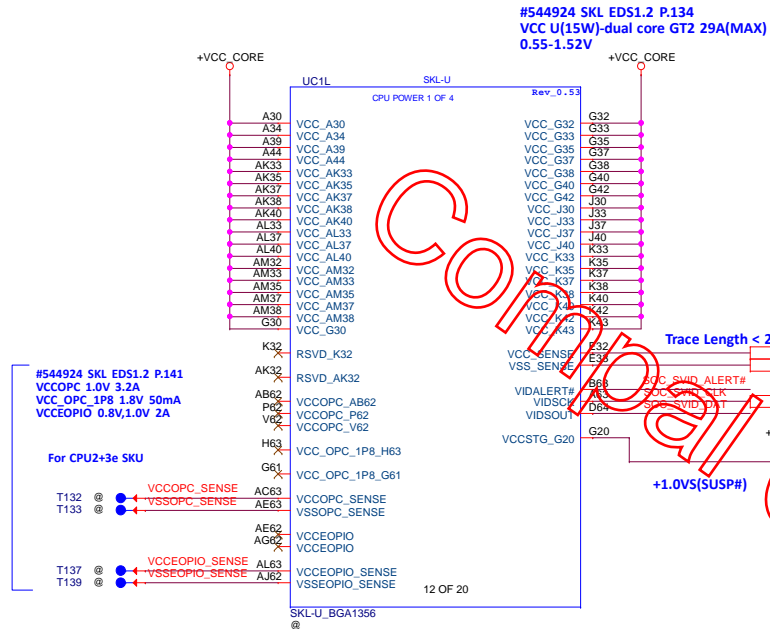
- When high DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL-U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
- When used as an interlock switch status input on this signal should be driven to 0 to indicate that the switch is closed and to 1 to indicate that the switch is open.
- If mechanical presence switches will not be used on the platform SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

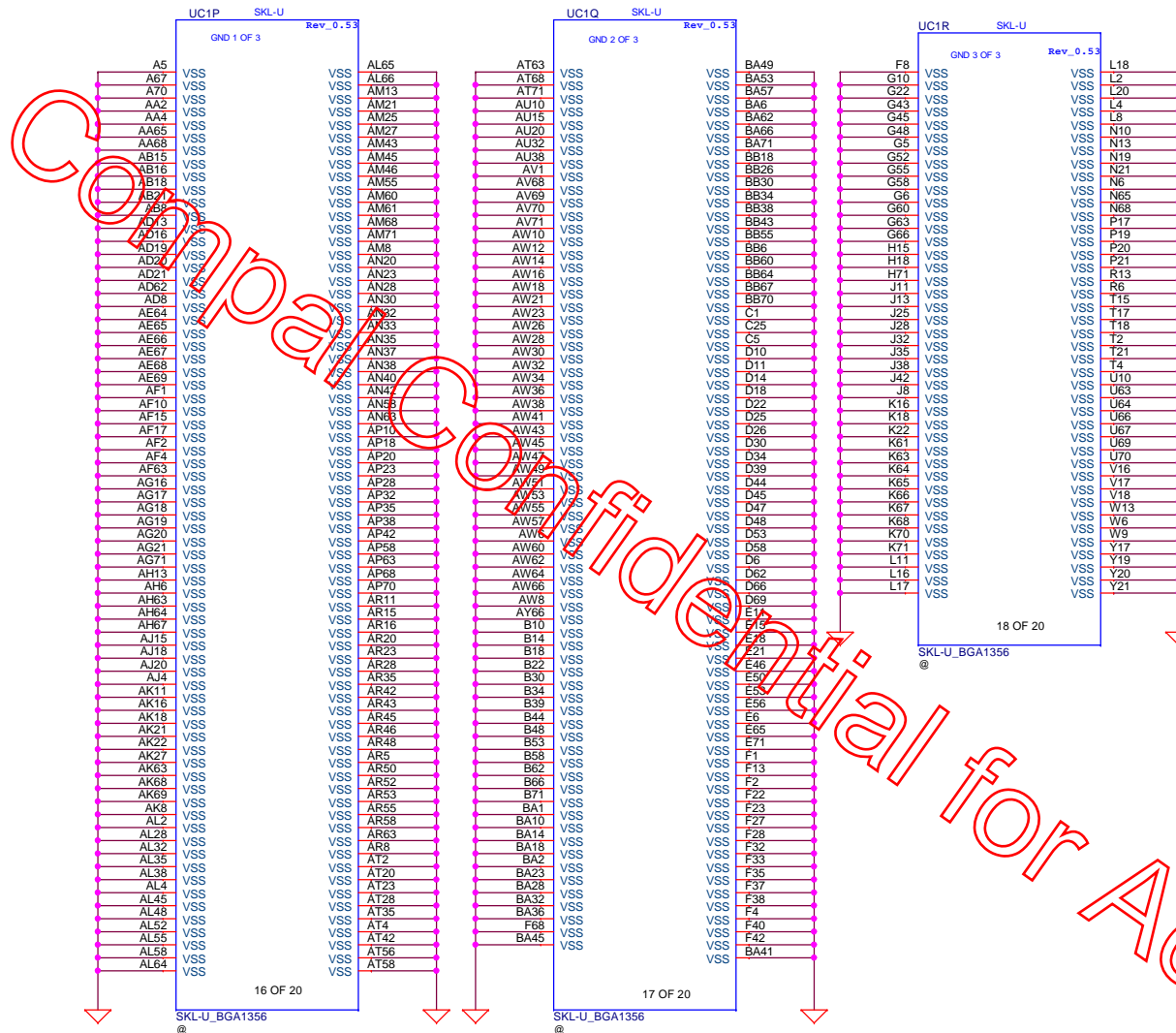


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				SKL-U(8/12)Power		
				Size	Document Number	Rev
				Custom	C5V01 M/B LA-E892P	1.A
Date:				Thursday, April 06, 2017	Sheet	14 of 57

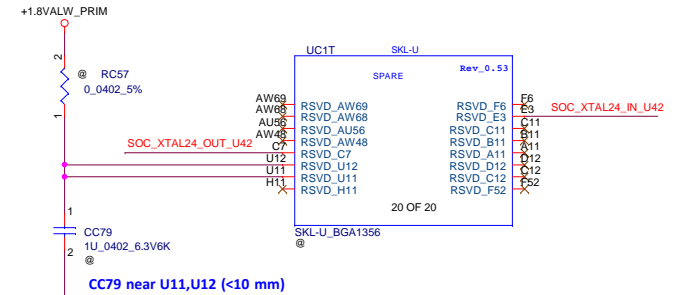
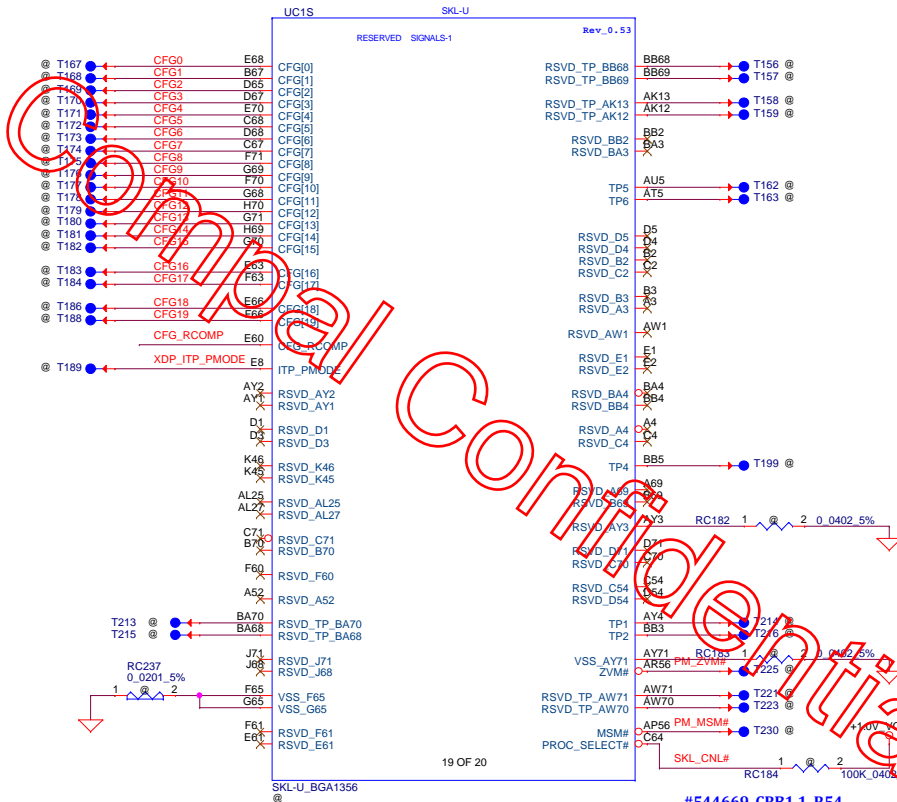


Processor Power Rails

Power Rail	Description	Control
VCCGT	Processor IA Cores Power Rail	SVID
VCCGT	Processor Graphics Power Rails	SVID
VCCGT	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VCCSA	System Agent Power Rail	SVID/Fixed (SKU dependent)
VCCIO	IO Power Rail	Fixed
VCCST	Sustain Power Rail	Fixed
VCCPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
VCCOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCOPC_1P8	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VCCEPIO	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



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								Size		Document Number		Rev	
								Custom		C5V01 M/B LA-E892P		1.A	
								Date:		Thursday, April 06, 2017		Sheet 17 of 57	

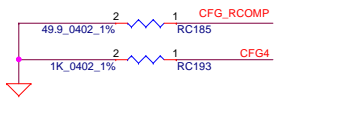


14MOW52, Connect U11, U12 to 1.8V for Cannonlake-U PCH compatibility

For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOP10 VR (connected only in 2 VR solution for OPC).



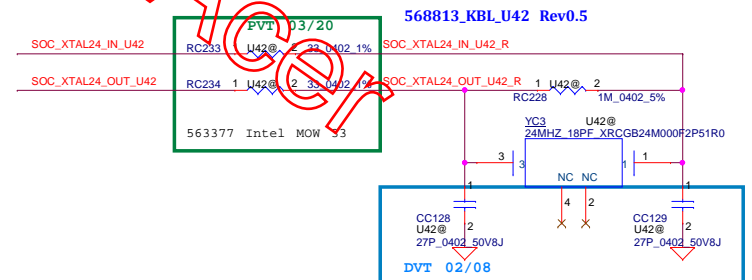
Display Port Presence Strap

CFG4

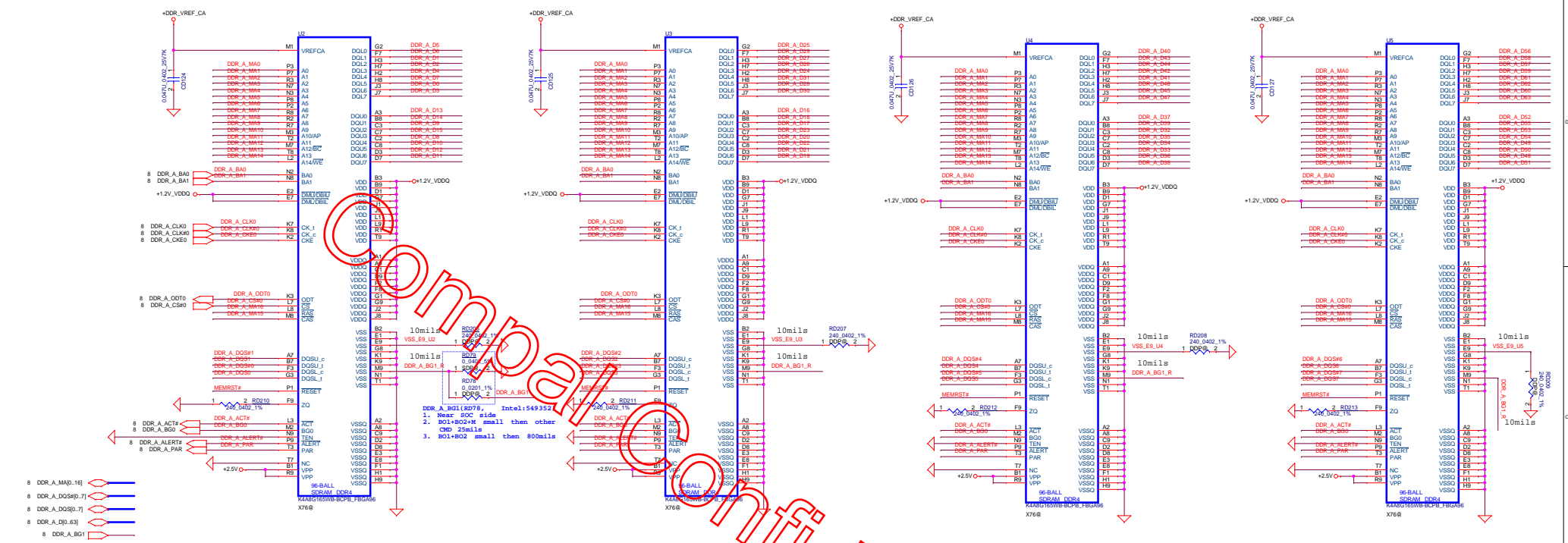
1 : Disabled; No Physical Display Port attached to Embedded Display Port

0 : Enabled; An external Display Port device is connected to the Embedded Display Port

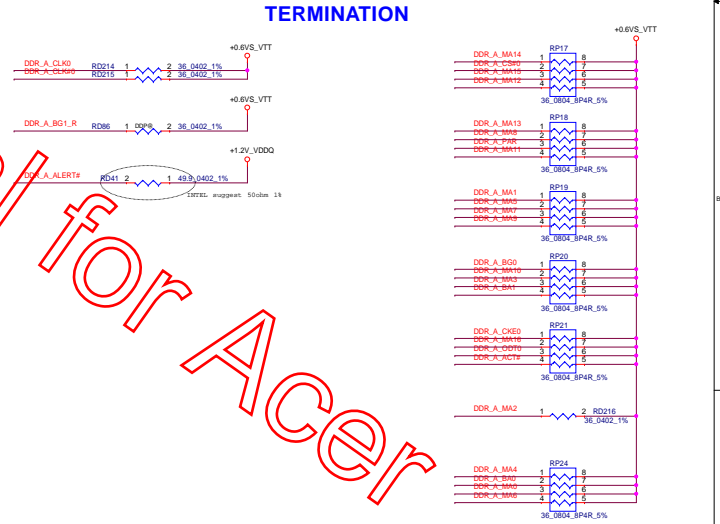
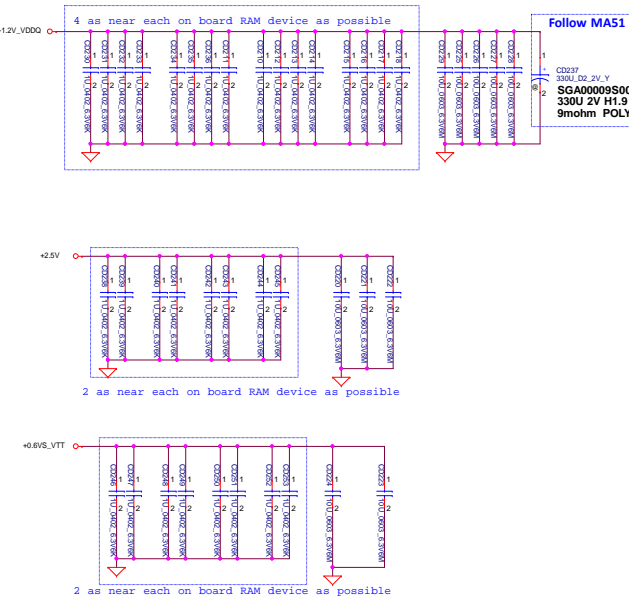
#544669 CRB1.1 P54
#544924 SKL EDS1.2 P125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.



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DDR4 mapping	SDP	DDP
E9	VSS	U2Q
M9	VSS	BG1
T7	NC	VSS
RCOMP(0) (SOC side)	200_1%	121_1%



Page 12	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hylix 4GB	0	0	0	0	SA000A1H20 (S IC D4 512M16 HSANB6NFR-UNC FBGA ABO1)
Micron 4GB	0	0	0	1	SA0009V220 (S IC D4 512M16 MT40A512M16Y-083E-B ABO1)
Samsung 4GB	0	0	1	0	SA0009U420 (S IC D4 512M16 KAABG165WB-BCRF FBGA 96P ABO1)
No Onboard Memory	1	1	1	1	No On Board Memory

GPIO	I/O	USAGE
GPIO0	O	GC6_FB_EN
GPIO1	O	MEM_VDD_CTL
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	3VS_MAIN_EN
GPIO6	I	GPU_EVENT#
GPIO7	O	3D_Vision
GPIO8	I	SYS_PEX_RST_MON#_R
GPIO9	IO	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	PWM_VID
GPIO12	I	PWR_LEVEL
GPIO13	O	PSI
GPIO14	I	HPD_A
GPIO15	I	HPD_C
GPIO16	I	FRAME_LOCK#
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F or HPD_B
GPIO20	Reserved	
GPIO21	O	GPU_PEX_RST_HOLD#
GPIO22		
GPIO23		

GPIO	I/O	USAGE
GPIO0	O	PWM_VID
GPIO1	O	GC6_FB_EN
GPIO2	I	GPU_EVENT#
GPIO3	IO	NVDDSS_PWM
GPIO4	O	1VS_MAIN_EN
GPIO5	I	FRAME_LOCK#
GPIO6	O	PSI
GPIO7	O	LCD_BL_PWM
GPIO8	O	MEM_VDD_CTL
GPIO9	IO	THERM_ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	LCD_VDD
GPIO12	I	PWR_LEVEL
GPIO13	O	LCD_BLEN
GPIO14	I	HPD_IFPA
GPIO15	I	HPD_IFPB
GPIO16	Reserved	
GPIO17	O	HPD_HPD
GPIO18	O	HPD_HPFE
GPIO19	O	3D_VISION
GPIO20	Reserved	
GPIO21	Reserved	
GPIO22	Reserved	
GPIO23	Reserved	

Table 15-8. I2CS Slave Address

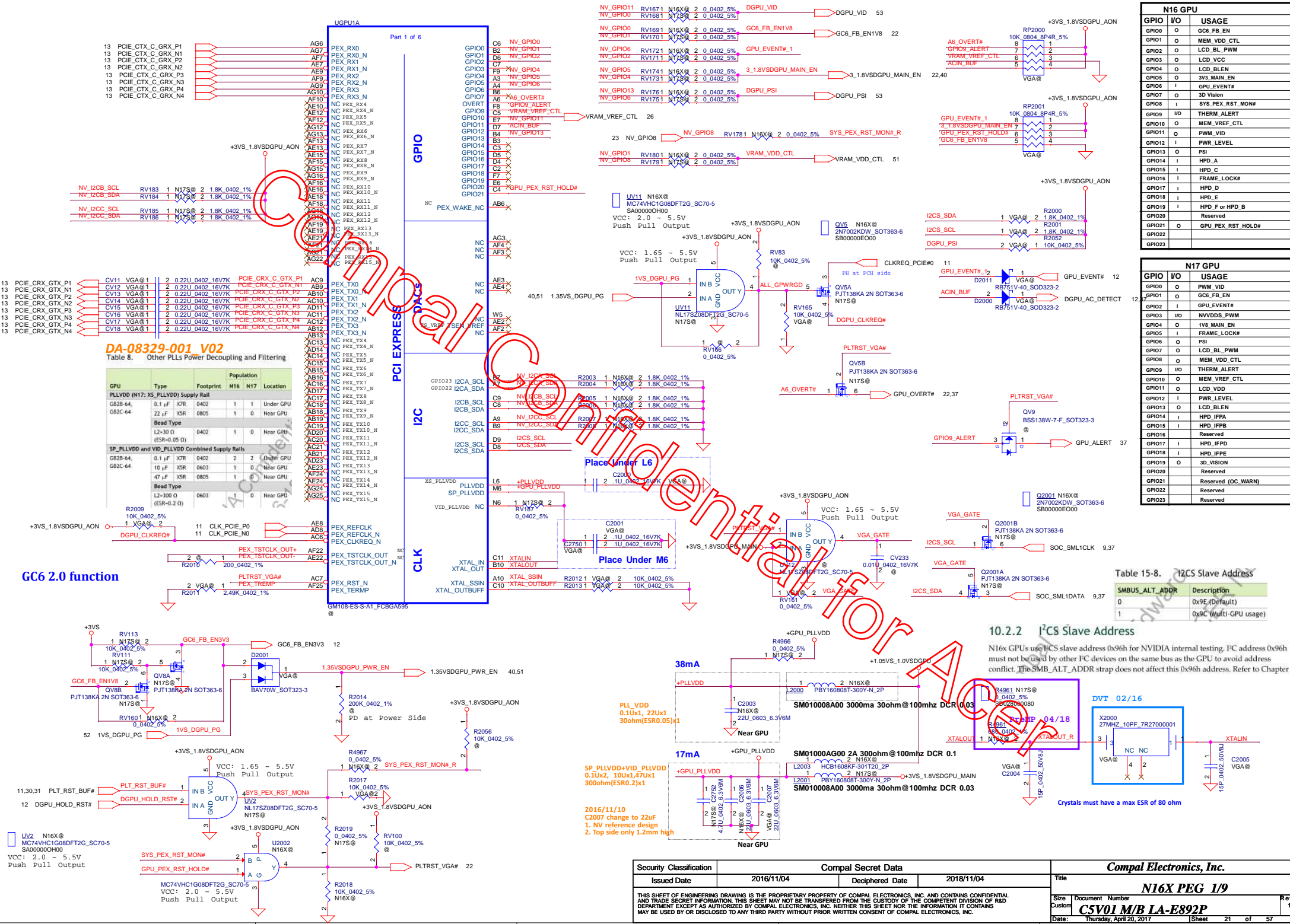
SMBUS_ALT_ADDR	Description
0	0x9C (Default)
1	0x9C (Multi-GPU usage)

10.2.2 I2CS Slave Address

N16X GPUs use I2CS slave address 0x96h for NVIDIA internal testing. I2C address 0x96h must not be used by other I2C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter

Crystals must have a max ESR of 80 ohm

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				Date:	Thursday, April 20, 2017
				Sheet	21 of 57

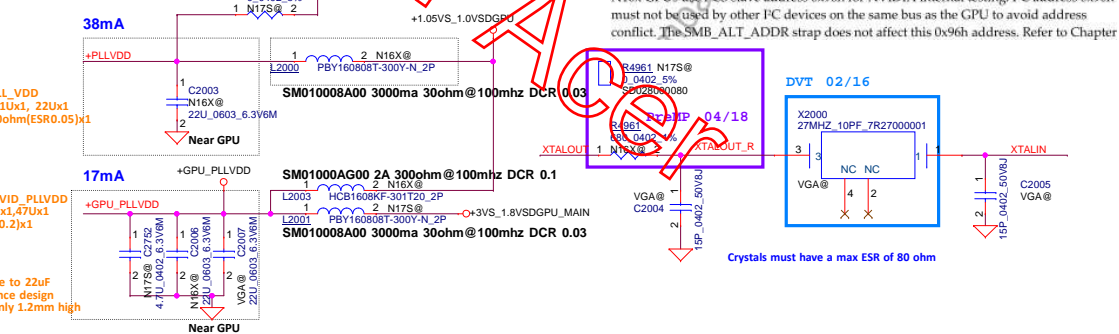
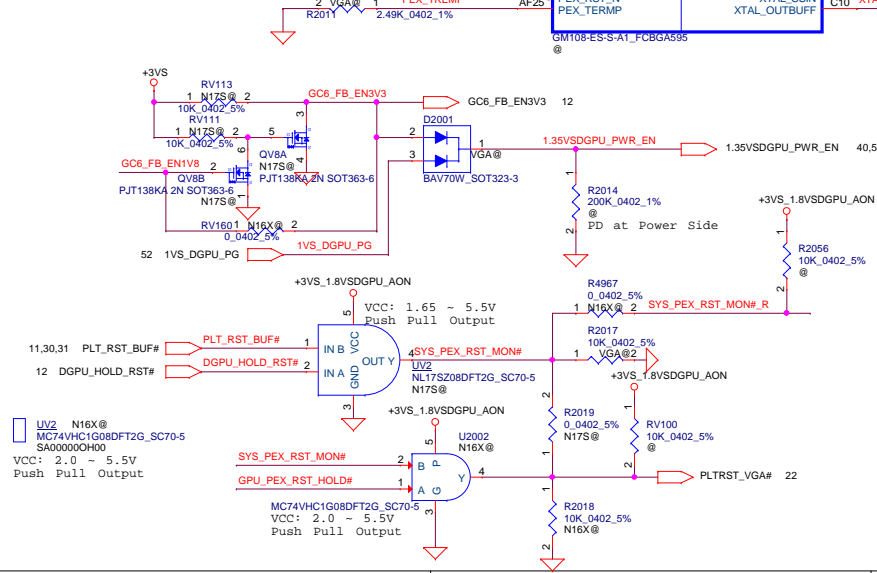


DA-08329-001_V02

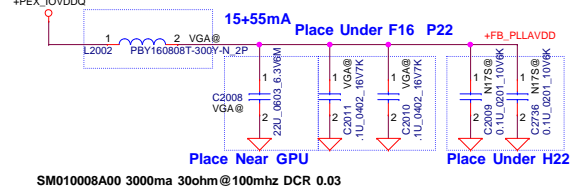
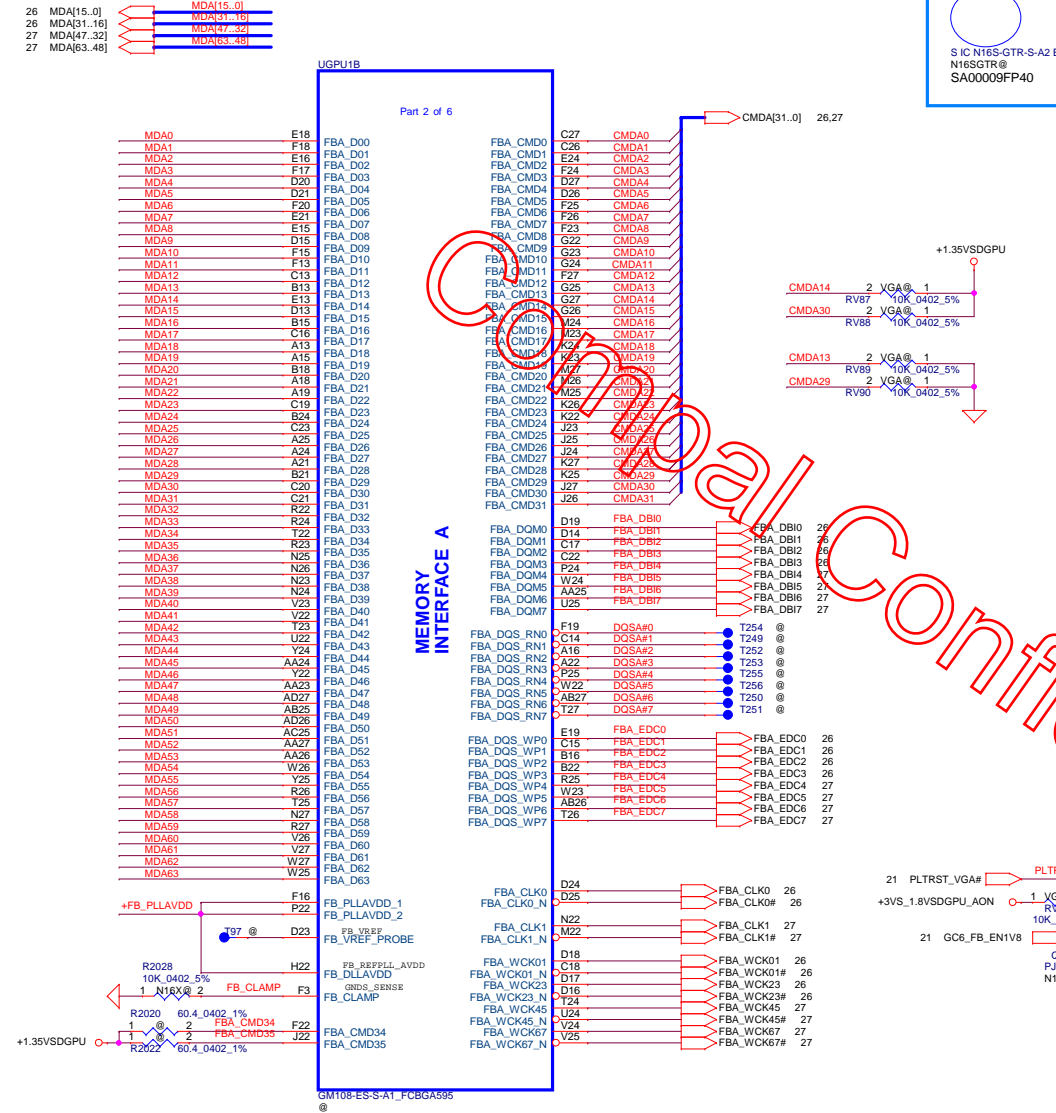
Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	Population	N16	N17	Location
PLLVD0 (N17: XS_PLLVD0) Supply Rail						
G82B-64, G82C-64	0.1 uF X7R 0402	1	1	Under GPU		
	22 uF X5R 0805	1	0	Near GPU		
SP_PLLVD0 and VID_PLLVD0 Combined Supply Rails						
G82B-64, G82C-64	0.1 uF X7R 0402	2	2	Under GPU		
	10 uF X5R 0603	1	0	Near GPU		
	47 uF X5R 0805	1	0	Near GPU		
	L2-300 0 (ESR<0.2 Ω)	0603	1	0	Near GPU	

GC6 2.0 function

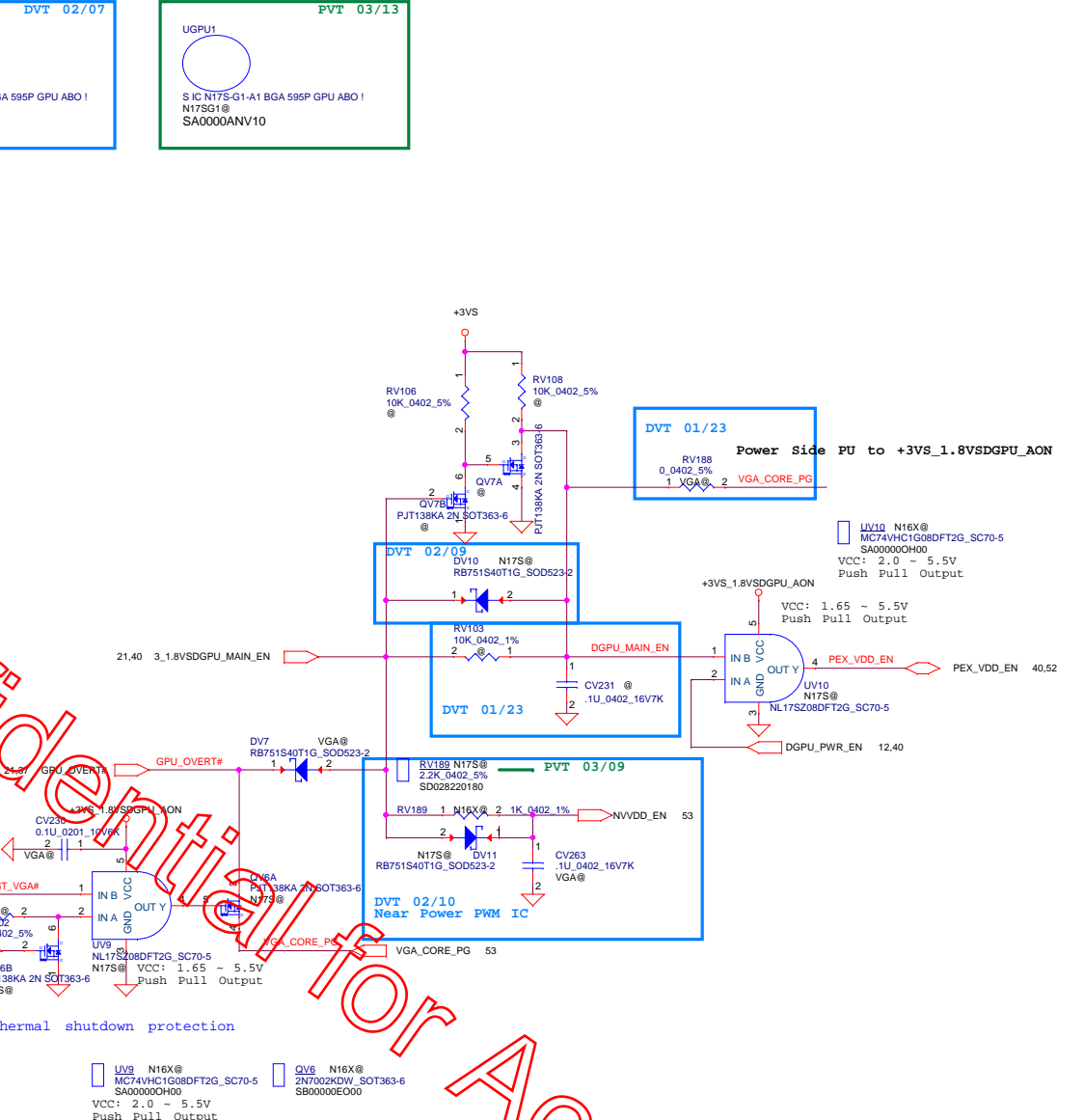


VRAM Interface



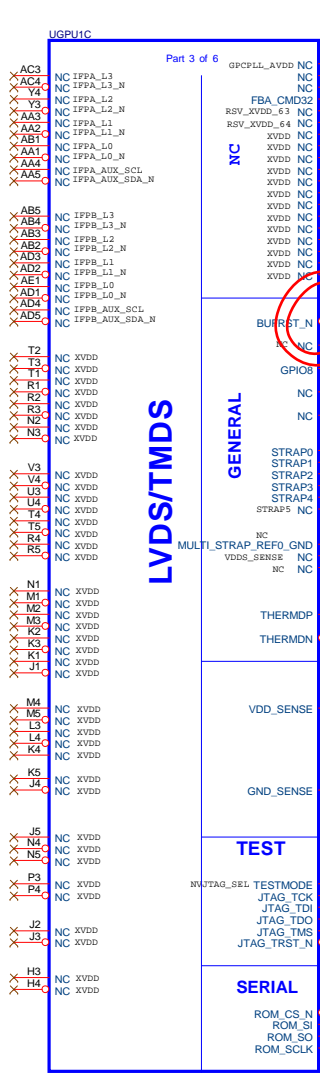
DA-08329-001 V01 Table 5. Frame Buffer PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
FB PLL Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 μF	X7R 0402	2	4	Under GPU
	22 μF	X6S 0805	1	1	Near GPU
Bead Type					
	30 Ω (ESR<0.010 Ω)	0603	1	1	Near GPU



NV 15x DG-06803-V03 NV 16x DG-07158-V04

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	FBX_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μF	X7R 0402	2	Under GPU
		22 μF	X5R 0805	1	Near GPU
		Bead Type			
		30 Ω (ESR<0.010 Ω)	0603	1	Near GPU

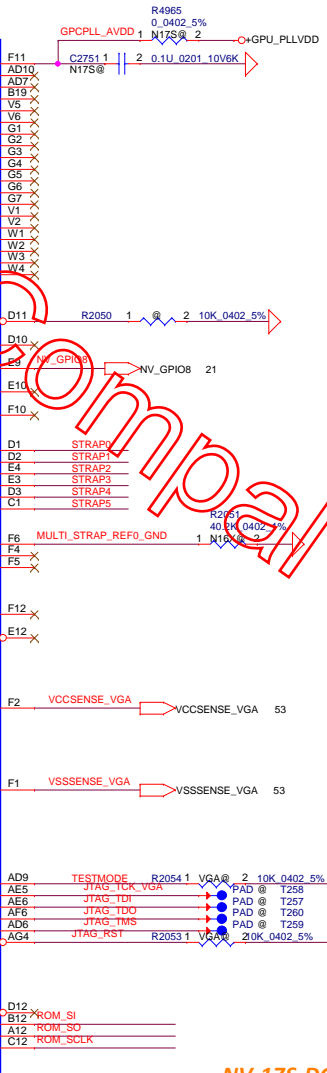


LVDS/TMDS

GENERAL

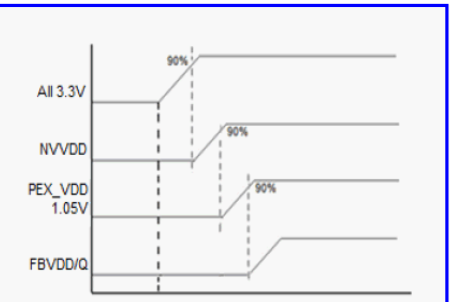
TEST

SERIAL



NV 17S DG-07785-001_V07

VGA Power Sequence (N16X)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

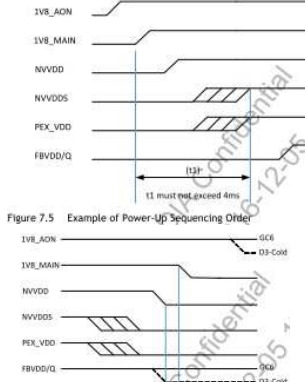
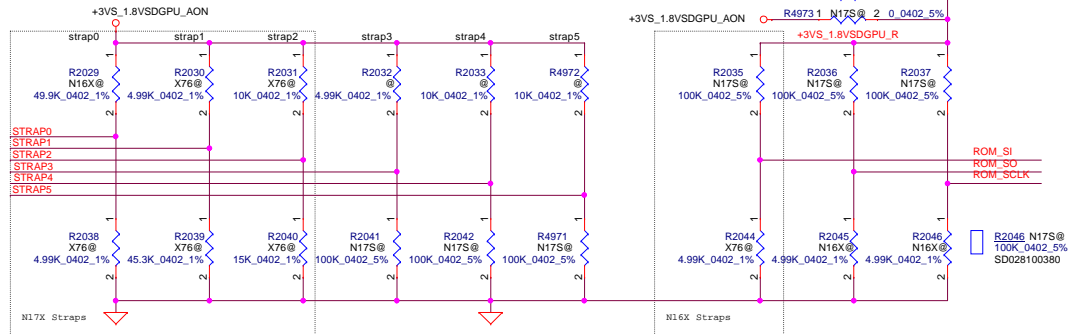


Figure 7.6 Example of Power-Down Sequencing Order

MULTI LEVEL STRAPS



Multi strap table

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N16S-GTR	+1.35V			2.5GHz	128Mx32x2 1G	0x7 (SA00009TT30) Samsung K4G41325FE-HC28 0x6 (SA000085V70) Hynix H5GC4H24AJR-T2C 0x3 (SA00007D880) Samsung K4G41325FC-HC03 0x4 () Micron	PU 49.9K	NC	NC	NC	NC	NC	PD 45.3K PD 34.8K PD 20K PD 24.9K	PD 4.99K	PD 4.99K
			X76739BOL04		256Mx32x2 2G	0x0 (SA000094R30) Samsung K4G80325FB-HC03 0x5(SA00009ZG20) Hynix H5GC8H24MJR-T2C 0x1 (SA000096K30) Micron MT51J256M32HF-60-A							PD 4.99K PD 30.1K PD 10K		

Decive ID : N16S-GTR 0x134D

Multi strap table

GPU	VRAM Voltage	RANK	X76	Freq	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	strap5	ROM_SI	ROM_SO	ROM_SCLK
N17S-G1	+1.35V			3.0GHz	128Mx32x2 1G	0x7 (SA00009TT30) Samsung K4G41325FE-HC28 0x6 (SA00008HQ10) Hynix H5GC4H24AJR-ROC 0x8 (SA00009E300) Micron EDW4032BAG-70-F-R	PU 100K	PU 100K	PU 100K						
			X76739BOL07		256Mx32x2 2G	0x0 (SA000092D00) Samsung K4G80325FB-HC28 0x2 (SA00009U110) Hynix H5GC8H24MJR-ROC 0x1 (SA00009TV10) Micron MT51J256M32HF-70-A	PD 100K	PD 100K	PD 100K				PU 100K	PU 100K	PU 100K
			X76739BOL08				PD 100K	PD 100K	PD 100K						
			X76739BOL09				PU 100K	PD 100K	PD 100K						

Decive ID : N17S-G1-A1 0x1D10

DA-08329-001_V02

Table 8. Other PLLs Power Decoupling and Filtering

GPU	Type	Footprint	N16	N17	Location
PLLVD0 (N17: XS_PLLVD0) Supply Rail					
GB2B-64	0.1 uF X7R 0402		1	1	Under GPU
GB2C-64	22 uF XSR 0805		1	0	Near GPU
Bead Type					
	L2=30 Ohm (ESR=0.05 Ohm)	0402	1	0	Near GPU
SP_PLLVD0 and VID_PLLVD0 Combined Supply Rails					
GB2B-64	0.1 uF X7R 0402		2	2	Under GPU
	10 uF XSR 0805		1	0	Near GPU
	47 uF XSR 0805		1	0	Near GPU
Bead Type					
	L2=300 Ohm (ESR=0.2 Ohm)	0603	1	0	Near GPU
NC (N17: GPCPLL_AVDD0) Supply Rail					
GB2C-64	0.1 uF X7R 0402		N/A	1	Under GPU
	4.7 uF X6S 0603		N/A	1	Near GPU
	22 uF X6S 0805		N/A	1	Near GPU
Bead Type					
	L2=90 Ohm (ESR=0.010 Ohm)	0603	N/A	1	Near GPU

NV 16x DG-07158-V05

Table 3-4. GPU Core Sensing Line Routing Constrains

Constraint Parameter	Requirement
Single-ended impedance	25 Ohm ± 10%
Differential Trace Impedance	50 Ohm ± 15%
Reference Plane	GND Reference
Routing Type	Stripline ¹ or Microstrip
Dielectric spacing	Stripline: ≥ 3.0x dielectric Microstrip: ≥ 4.0x dielectric
Intrapair skew	≤ 5 ps
Via stub	
Trace length	GPU to R ₁ /R ₂ ≤ 250 mm (9842.5 mil) R ₁ /R ₂ to VR ≤ 50 mm (1968.5 mil)
Note:	
1. Stripline is recommended to minimize EMI. Do not route over any voids.	

Table 3-5. Resistance Mapping to Vex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kOhm	1000	0000
10.0 kOhm	1001	0001
15.0 kOhm	1010	0010
20.0 kOhm	1011	0011
24.9 kOhm	1100	0100
30.1 kOhm	1101	0101
34.8 kOhm	1110	0110
45.3 kOhm	1111	0111

NV 16x DG-07158-V05

Table 3-9. DDR3 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/GB2-64 DDR3	0.1 μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU

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Table 4. Frame Buffer Core and IO Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
FBVDD/Q Supply Rail for GDDR5						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	2	0	Under GPU
	1 µF	X7R	0603	2	8	Under GPU
	4.7 µF	X6S	0603	2	0	Under GPU
	10 µF	X6S	0603	0	2	Under GPU
	10 µF	X6S	0603	1	1	Near GPU
	22 µF	X6S	0603W	1	3	Near GPU

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Table 3-16. PEX_IOVDD/Q Power Rail Combined

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

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Table 7-13. Default GPU Drive Calibration for Frame Buffer Interface

Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
GDDR5/BGA-170	1.35V or 1.50V	40.2Ω	40.2Ω	60.4Ω

NV 16x DG-07158-V05

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
GB4B-128		1 µF	X5R	0603	1	1	Near GPU
GB3-256		4.7 µF	X5R	0603	1	1	Near GPU

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Table 9. VDD_AON and VDD_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
N16 3V3_MAIN (N17 VDD18) Supply Rail						
GB2B-64,	0.1 µF	X7R	0402	2	2	Under GPU
GB2C-64	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU
N16 3V3_AON (N17 VDD_AON) Supply Rail						
GB2B-64,	0.1 µF	X7R	0402	1	1	Under GPU
GB2C-64	1.0 µF	X6S	0603	1	1	Near GPU
	4.7 µF	X6S	0603	1	1	Near GPU

NV 16x DG-07158-V05

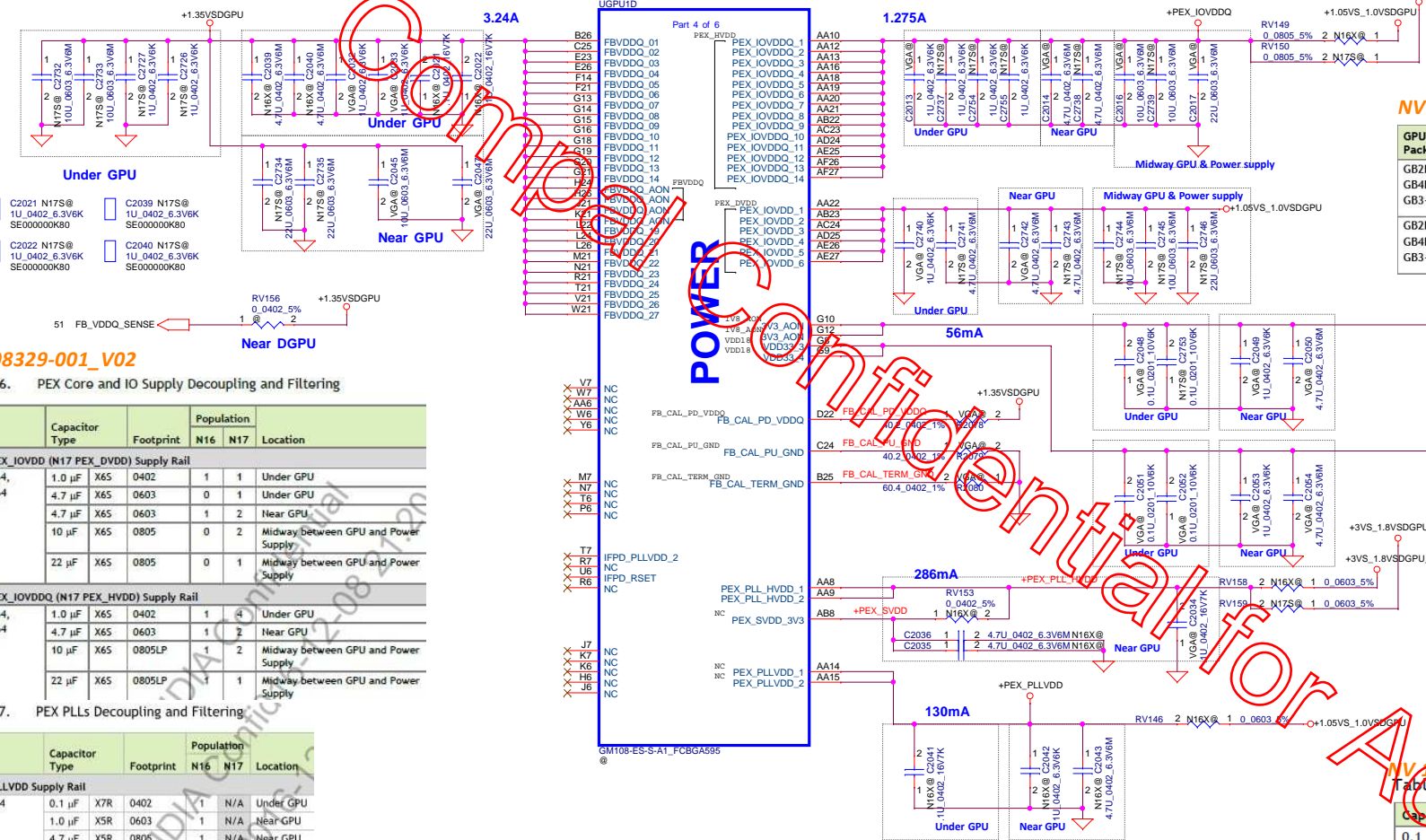
Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type		Footprint	Population	Location
0.1 μF	X7R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

NV 16x DG-07158-V05

Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 µF X7R	0402	1	Under GPU
1.0 µF X5R	0603	1	Near GPU
4.7 µF X5R	0805	1	Near GPU



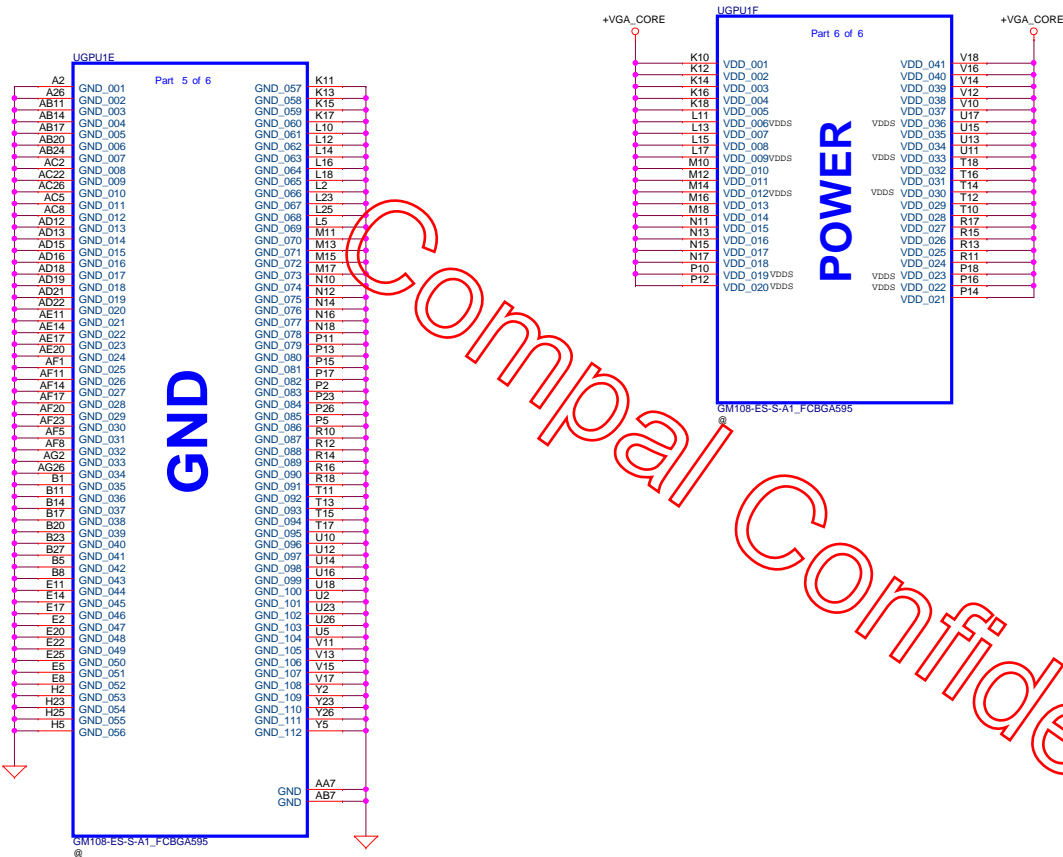
DA-08329-001_V02

Table 6. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	1	Under GPU
	4.7 µF	X6S	0603	0	1	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805	0	2	Midway between GPU and Power Supply
	22 µF	X6S	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 µF	X6S	0402	1	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X6S	0805LP	1	2	Midway between GPU and Power Supply
	22 µF	X6S	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
PEX_PLLVDD Supply Rail						
GB2B-64	0.1 µF	X7R	0402	1	N/A	Under GPU
	1.0 µF	X5R	0603	1	N/A	Near GPU
	4.7 µF	X5R	0805	1	N/A	Near GPU
PEX_SVDD_3V3 Supply Rail						
GB2B-64	4.7 µF	X5R	0603	2	N/A	Near GPU
PEX_PLL_HVDD Supply Rail						
GB2B-64, GB2C-64	0.1 µF	X7R	0402	1	1	Near GPU



NV 16x DG-07158-V05

Table 3-6. NVVDD Decoupling Footprint and Population

GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64 / GB2-64	4.7 μ F	X6S 0603	10	10	Under GPU
	1 μ F	X6S 0402	4	4	Under GPU
	47 μ F	X5R 0805	1	1	Near GPU
	22 μ F	X5R 0805	1	1	Near GPU
	4.7 μ F	X5R 0805	5	5	Near GPU
	330 μ F	POS 7343	1	1	Near GPU ESR \leq 6 m Ω

DA-07750-000-V02

Table 6. EDP-Continuous³

Products	VRAM Type	GPU Core		GPU FBIO		FB Total ^{1,5}		1.05V Total ²	1.05V ⁴	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06		
	DDR3/L	21.0	1.4	2.4	2.3	0.80	0.06			
N165-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06		
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06		
	DDR3/L	26.0	1.4	2.4	2.3	0.80	0.06			

Table 7. EDP-Peak³

Products	VRAM Type	GPU Core		GPU FBIO		FB Total ^{1,5}		1.05V Total ²	1.05V ⁴	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1			
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1			
N165-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1			
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1			
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1			

DA-07751-000-V02

Table 5. EDP-Continuous³

Product	VRAM Type	GPU Core		GPU FBIO		FB Total ^{1,5}		1.05V Total ²	1.05V ⁴	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR1	GDDR5 @ 2.0 GHz	18.5	—	2.0	—	4.2	0.8	0.06		
	GDDR5 @ 2.5 GHz	18.5	—	2.0	—	4.7	0.8	0.06		
	DDR3/L	19.0	1.4	1.4	2.4	2.3	0.8	0.06		

Table 6. EDP-Peak³

Products	VRAM Type	GPU Core		GPU FBIO		FB Total ^{1,5}		1.05V Total ²	1.05V ⁴	3.3V Total
		(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR1	GDDR5 @ 2.0 GHz	30.0	—	2.9	—	6.8	2.1			
	GDDR5 @ 2.5 GHz	31.0	—	3.1	—	7.2	2.1			
	DDR3/L	28.5	2.6	2.3	4.1	3.9	2.1			

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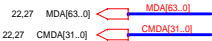
Table 7. Output EDP-Continuous

Product	NVVD	GPU FBIO	FB Total ⁵	1.0V Total ¹	1.8V Total ²
	(A)	(A)	(A)	(A)	(A)
N175-G1	30.0	2.0	3.4	0.1	0.3

Table 8. Output EDP-Peak

Product	NVVD	GPU FBIO	FB TOTAL ⁴	1.0V Total ¹
	(A)	(A)	(A)	(A)
N175-G1	60.1	3.2	6.6	0.2

VRAM GDDR5 chips



X76 for N16X 2G VRAM



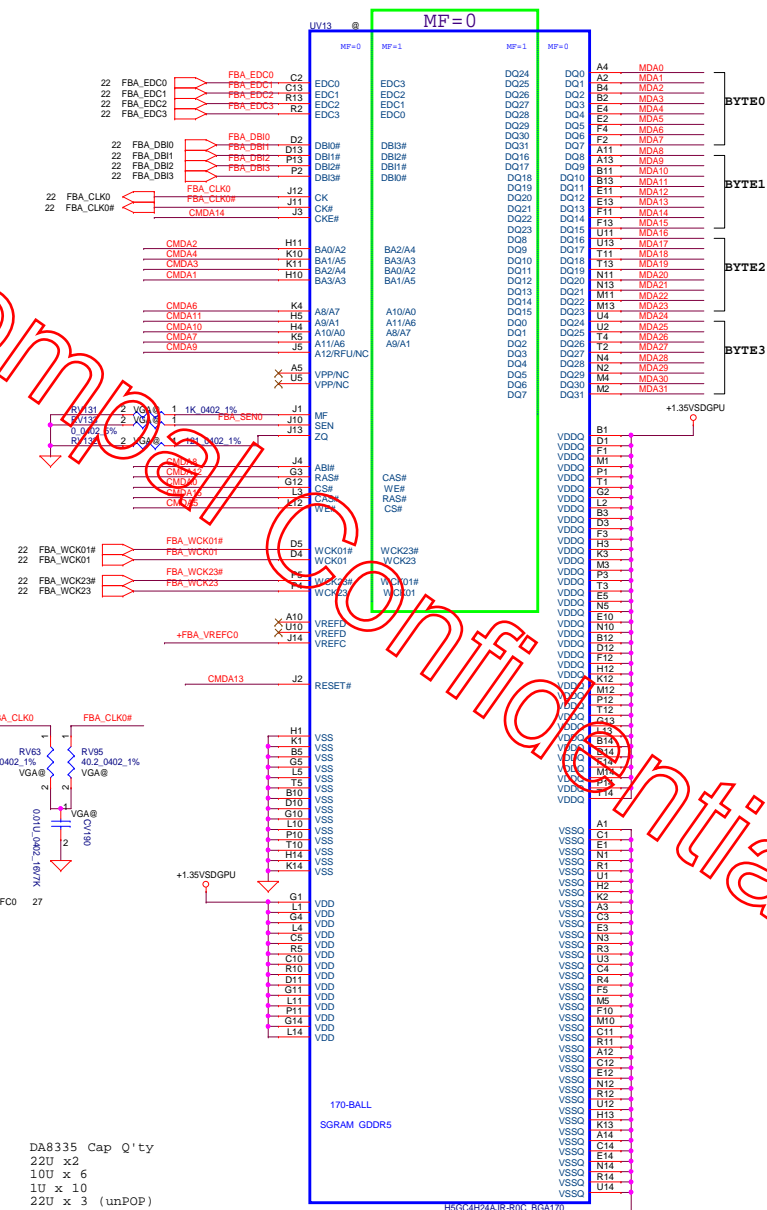
X76 for N17S 2G VRAM

DVT 02/07



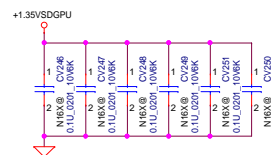
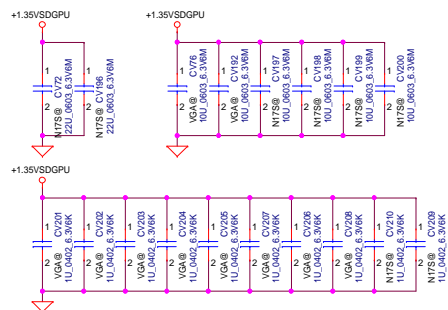
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Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	AB1#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		AB1#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

Channel 0 BOT SIDE



DA8335 Cap Q'ty
22U x2
10U x 6
1U x 10
22U x 3 (unPOP)

```
N16X Cap Q'ty
10U x2
1U x 8
0.1U x 6
```



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title	N16X Lower Rank0 6/9	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	
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				Date:	Thursday, April 05, 2017	Sheet 26 of 57

VRAM GDDR5 chips GDDR5 Mode H Mapping

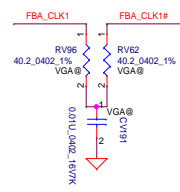
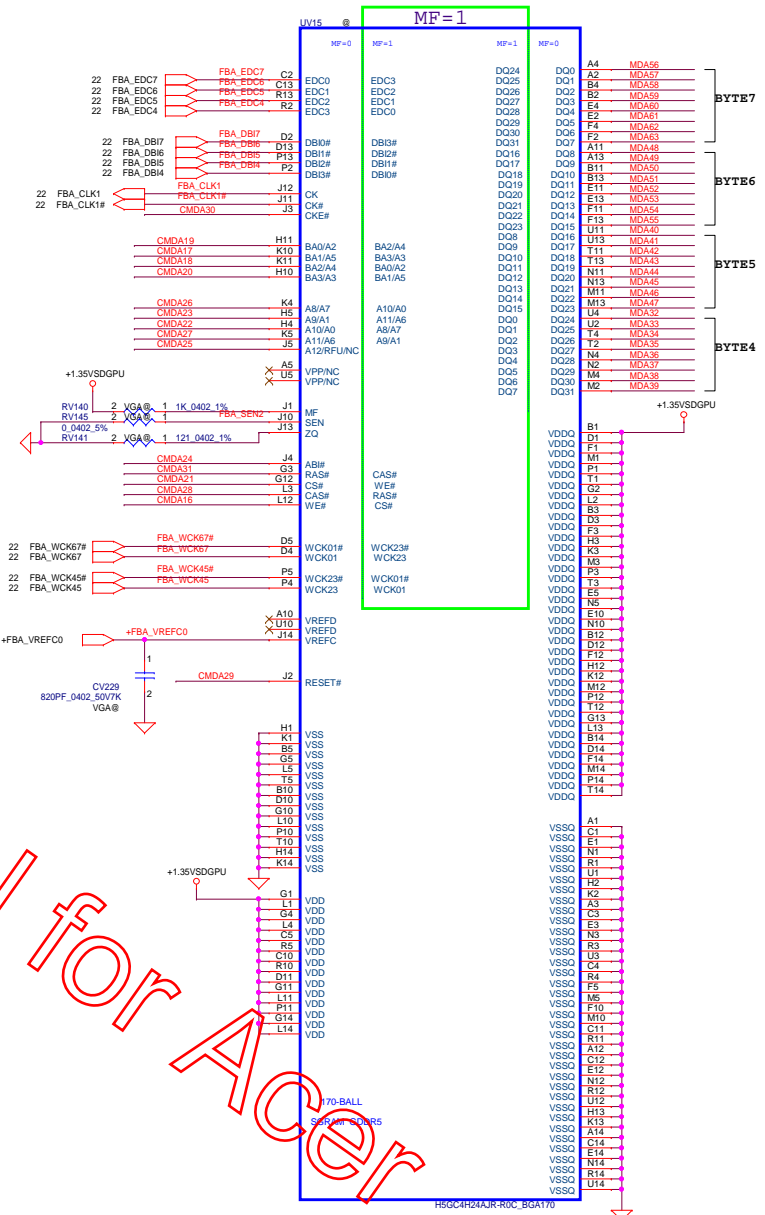
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22.26 CMDA[31..0] CMDA[31..0]

	DATA Bus
Address	0..31 32..63
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	AB1#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CAS#
CMD16	CS#
CMD17	A3_BA3
CMD18	A2_BA0
CMD19	A4_BA2
CMD20	A5_BA1
CMD21	WE#
CMD22	A7_A8
CMD23	A6_A11
CMD24	AB1#
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CMD28	RAS#
CMD29	RST#
CMD30	CKE#
CMD31	CAS#

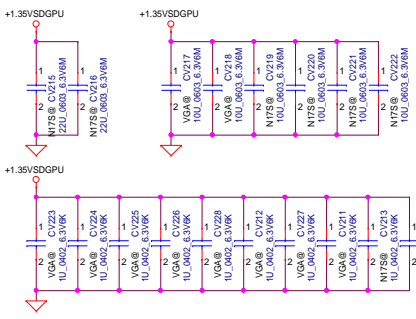
Compal Confidential for Acer

Channel 1 BOT SIDE

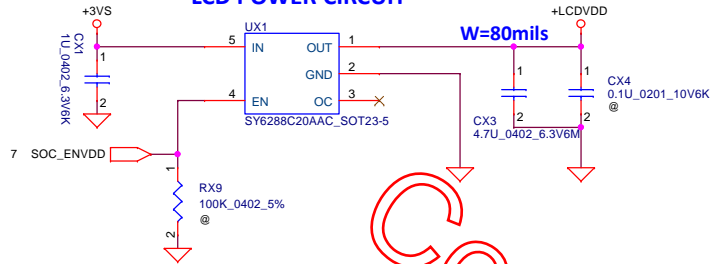


DA8335 Cap Q'ty
 22U x2
 10U x 6
 1U x 10
 22U x 3 (unPOP)

N16X Cap Q'ty
 10U x2
 1U x 8
 0.1U x 6



LCD POWER CIRCUIT

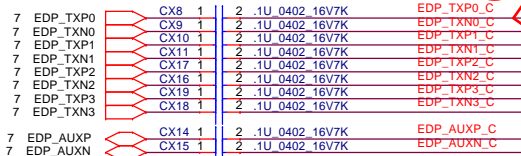
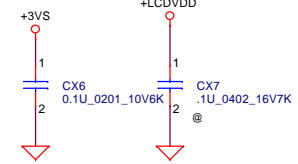


W=60mils

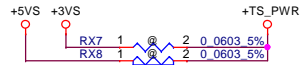
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220ohm@100mhz
DCR 0.04

Note: Unmount LX1 when panel boost circuit was use. (2S battery cell)

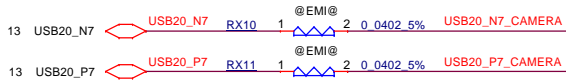
Place closed to JEDP1



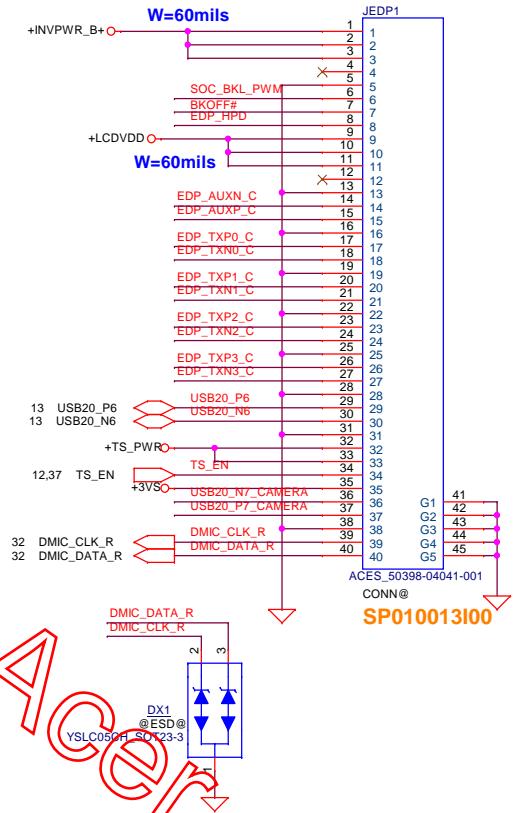
Touch Screen



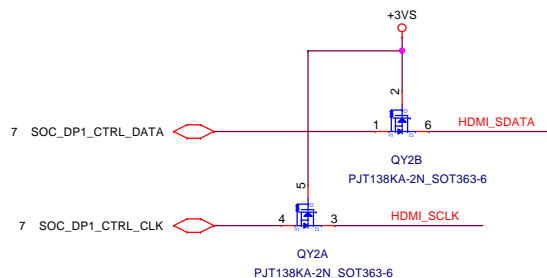
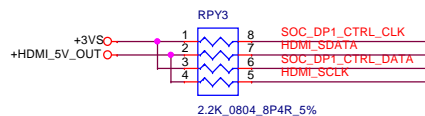
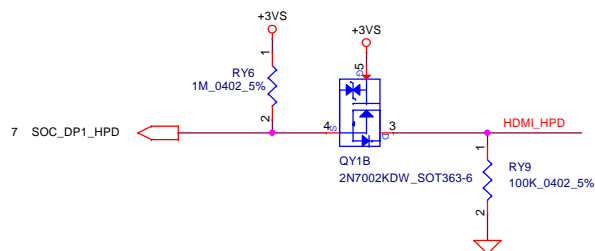
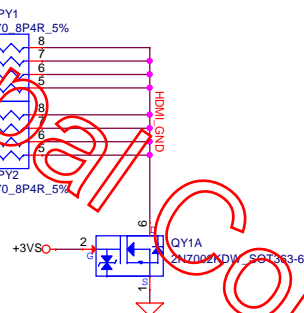
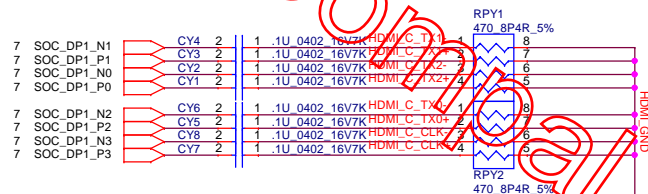
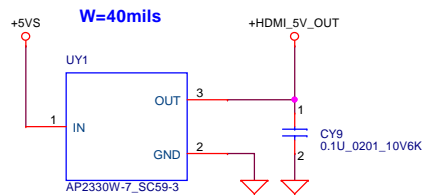
Camera



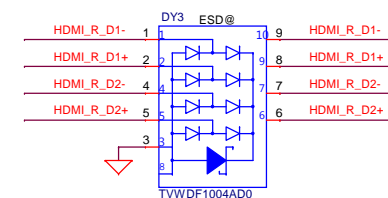
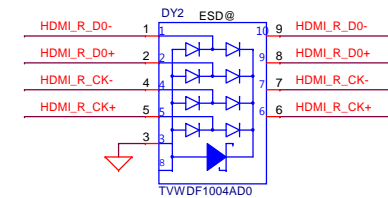
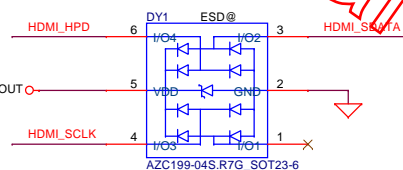
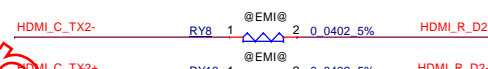
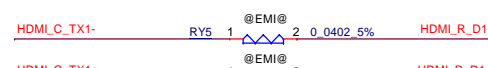
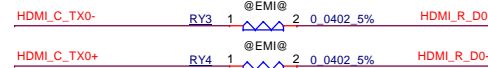
LED PANEL Conn.



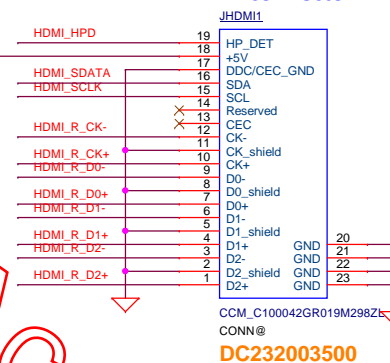
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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Date: Thursday, April 06, 2017				C5V01 M/B IA-E892P				Document Number			
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Intel spec Ron/Cout : 3ohm/10pF.
SB000016K00, S TR PJT138KA 2N SOT363-6

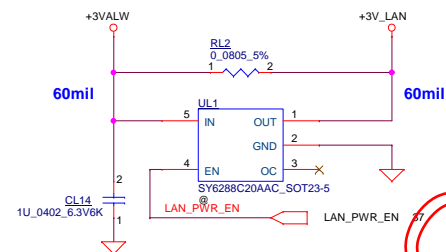


HDMI connector

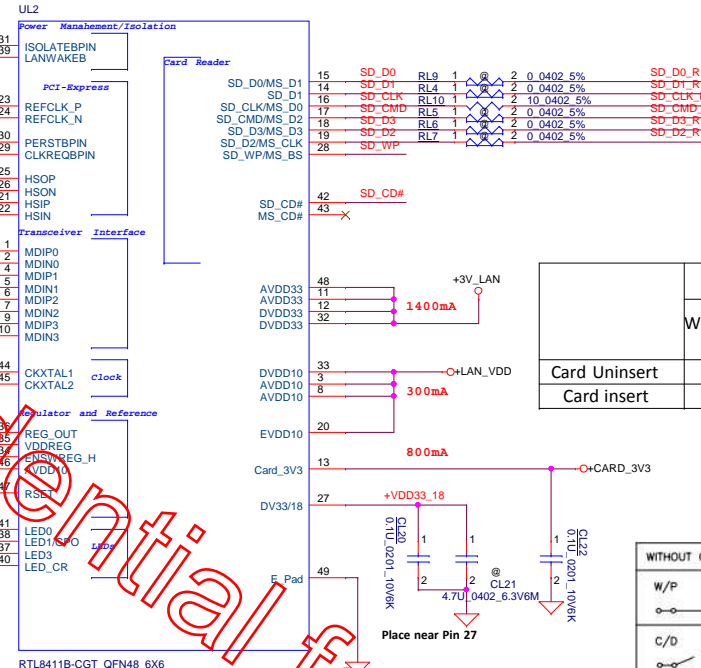
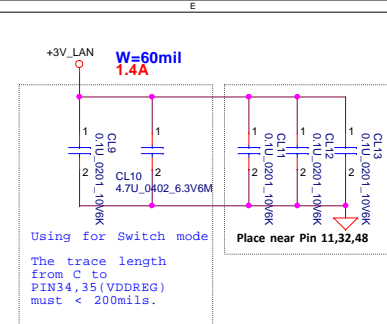
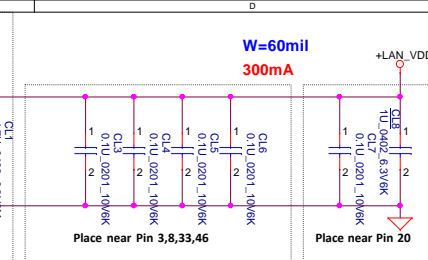
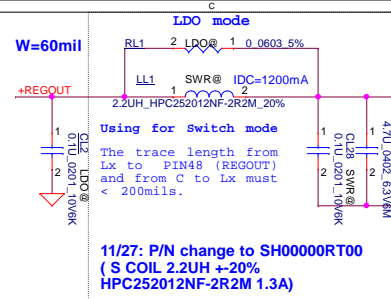
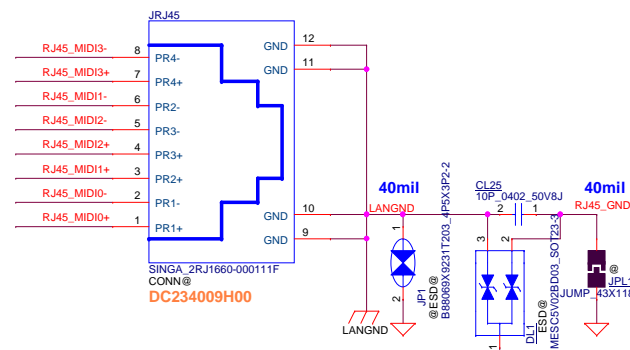
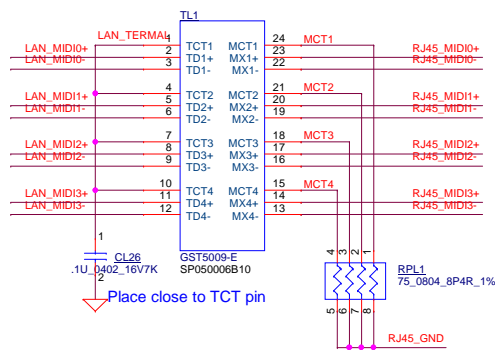
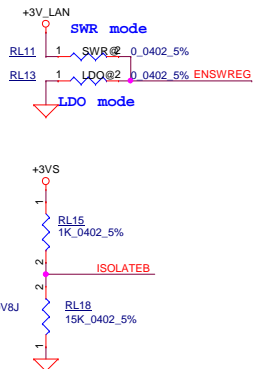
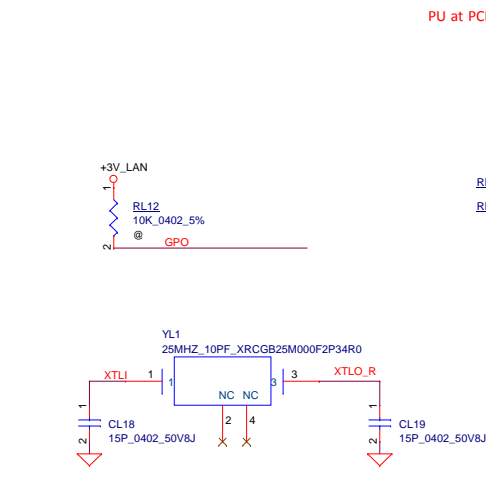


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Size	Document Number	Rev		1.A	
Custom	C5V01 M/B 1A-E892P	Date:		Thursday, April 06, 2017	
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LAN-RTL8411B



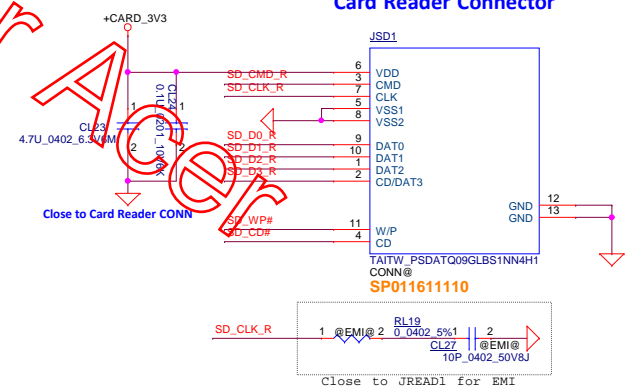
```
From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5-2.8A
+3V_LAN Rising time must >0.5ms and <100ms
```



	Protect cotact		Card contact
	Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open	Open
Card insert	Open	Close	Close

WITHOUT CARD	CARD INSERTED-LOCK	CARD INSERTED-UNLOCK
<p>W/P GND</p>	<p>W/P GND</p>	<p>W/P GND</p>
<p>C/D VSS1 P3</p>	<p>C/D VSS1 P3</p>	<p>C/D VSS1 P3</p>

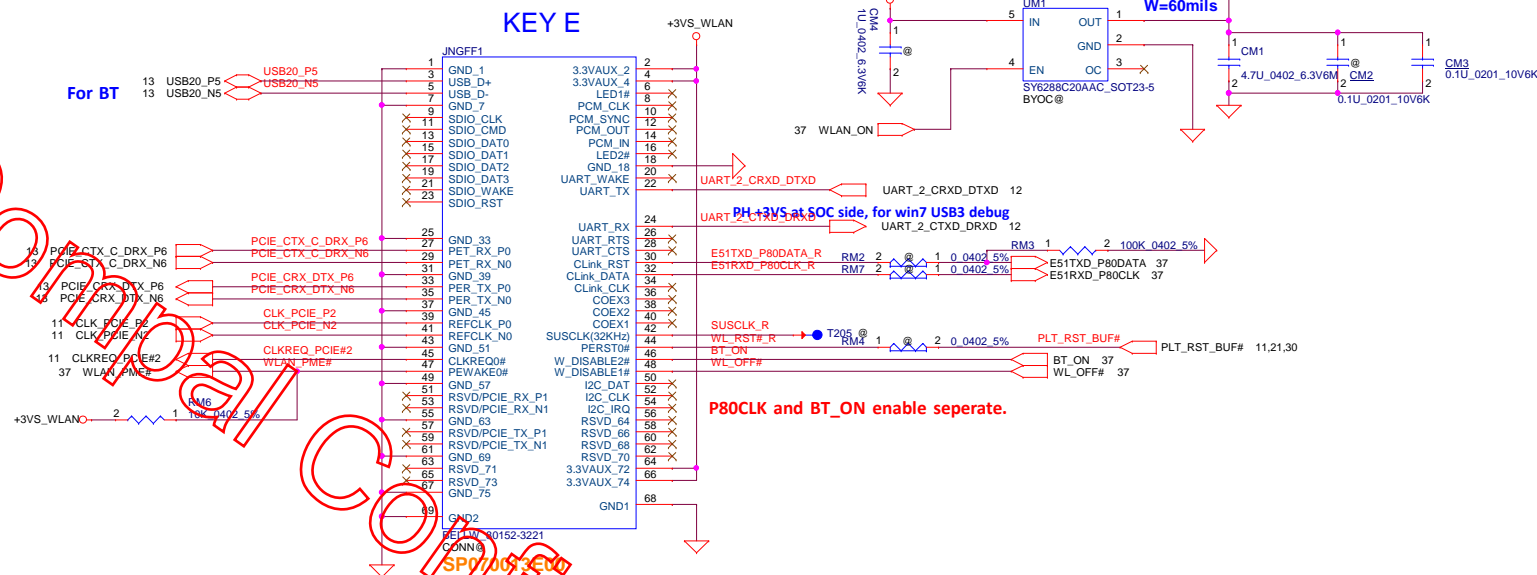
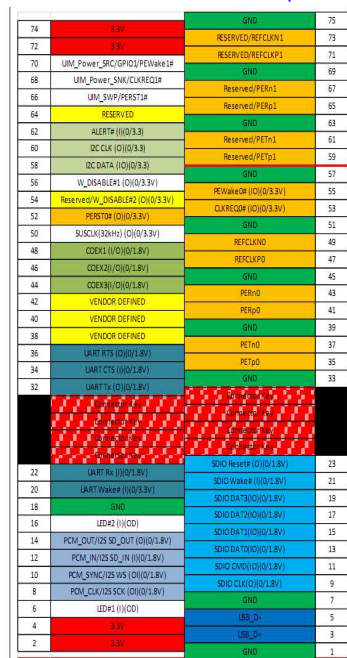
Card Reader Connector



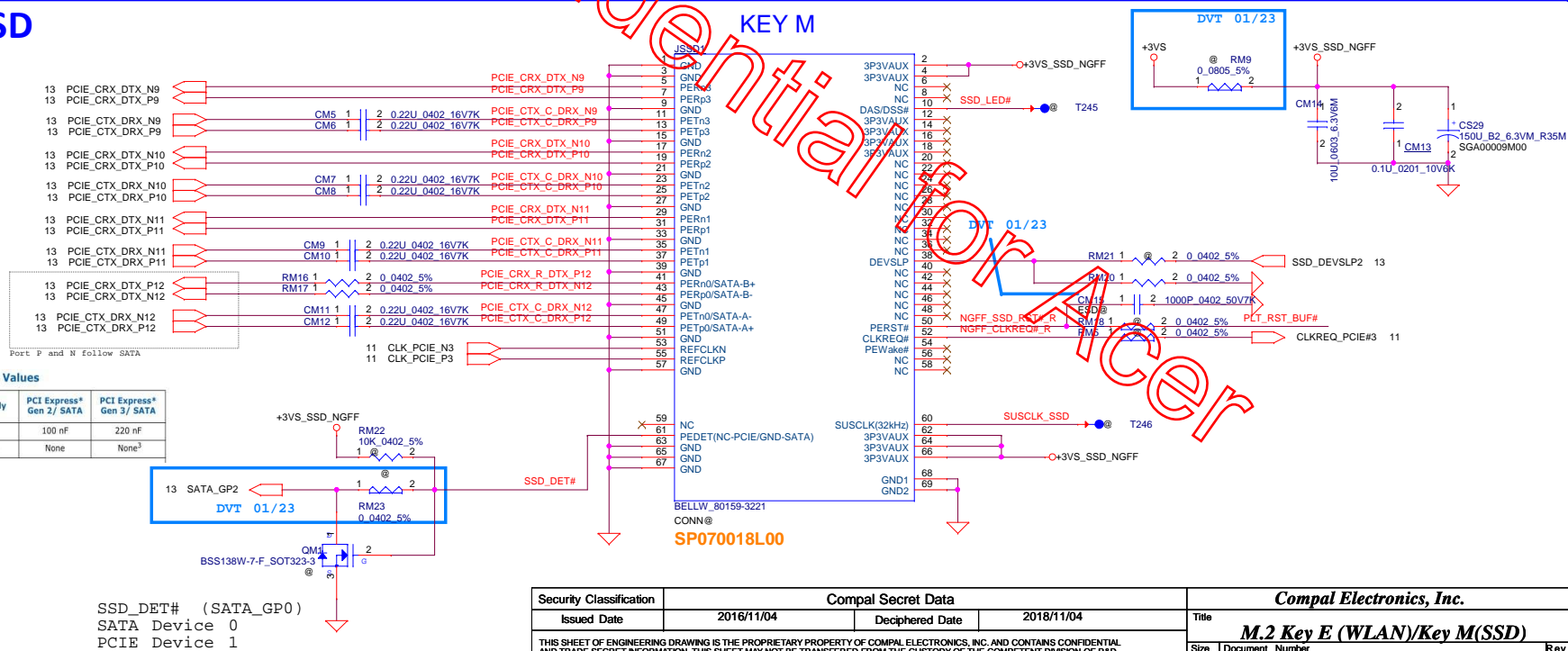
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Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title	LAN RTL8411B	
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Wireless LAN

NGFF WL+BT (KEY E)



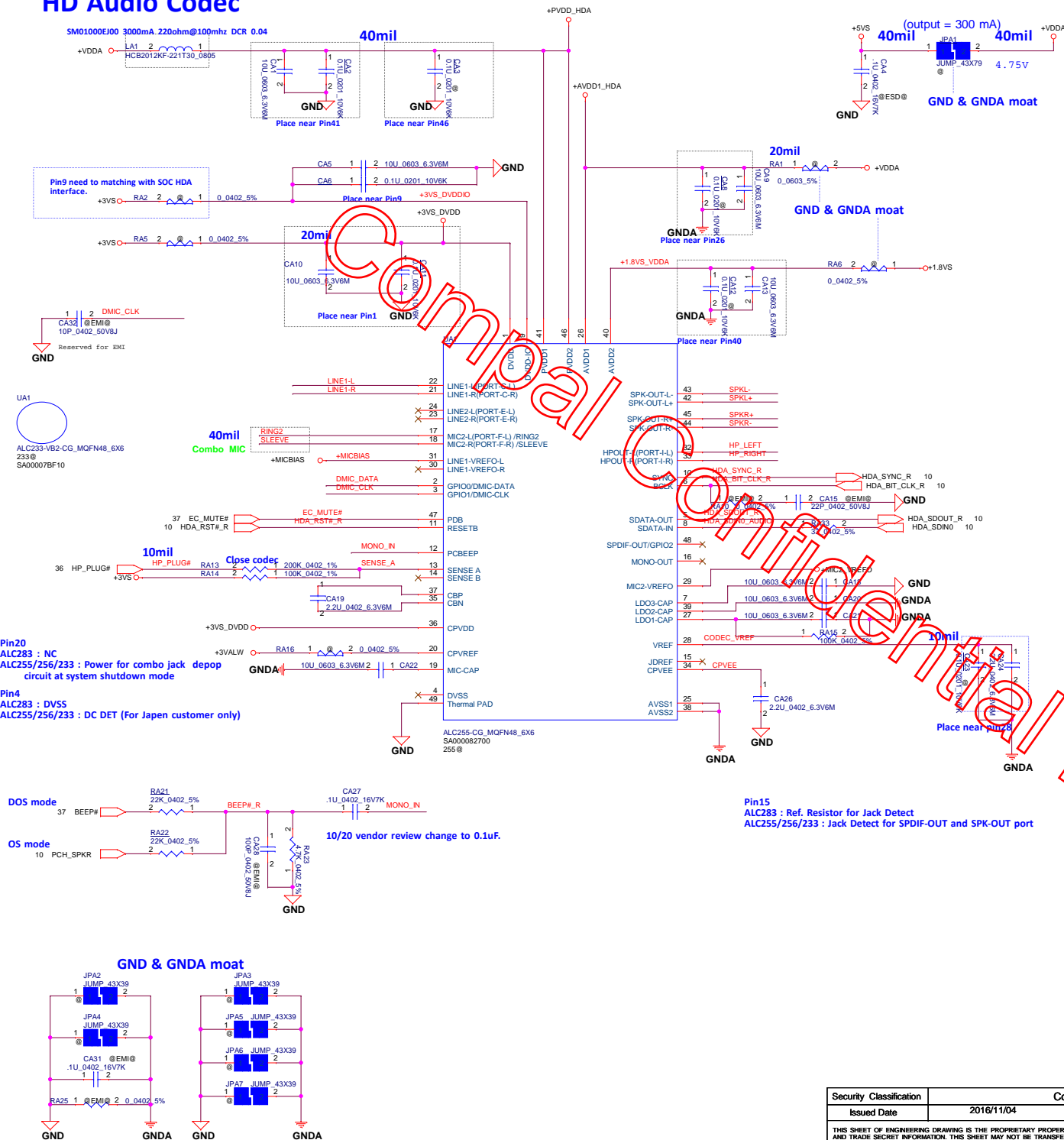
mSATA/SSD

Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

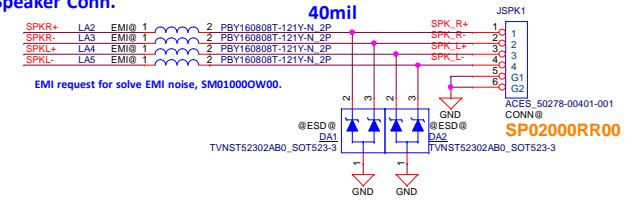
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

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				Custord	C5V01 M/B LA-E892P	1A
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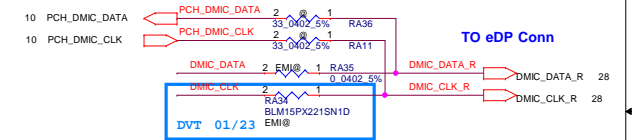
HD Audio Codec



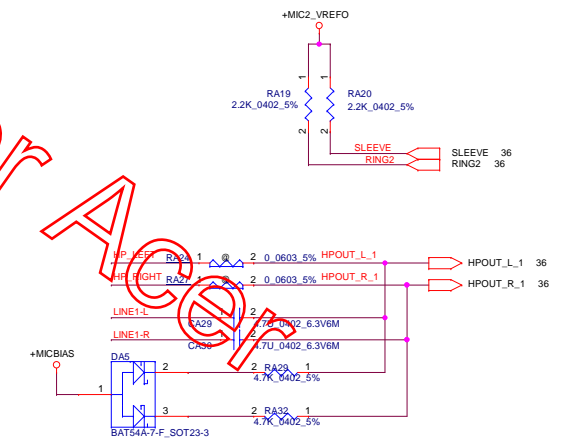
Int. Speaker Conn.



Digital MIC



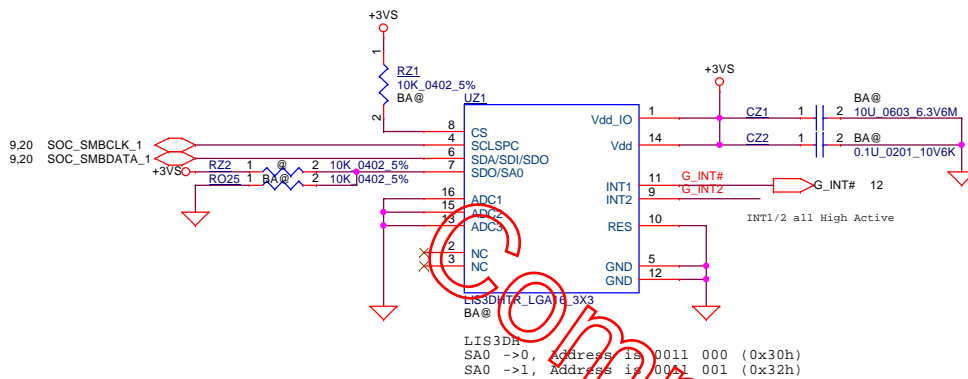
Headphone Out



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2016/11/04		Deciphered Date		2018/11/04		Title		HD Audio Codec ALC255/ALC233 Colay	
Size		Document Number		Customer		CSV01 M/B LA-E892P		Date:		Thursday, April 06, 2017	
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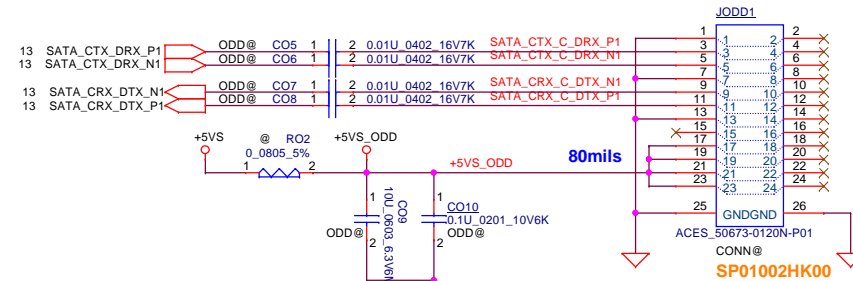
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G-Sensor reserved for BA serial

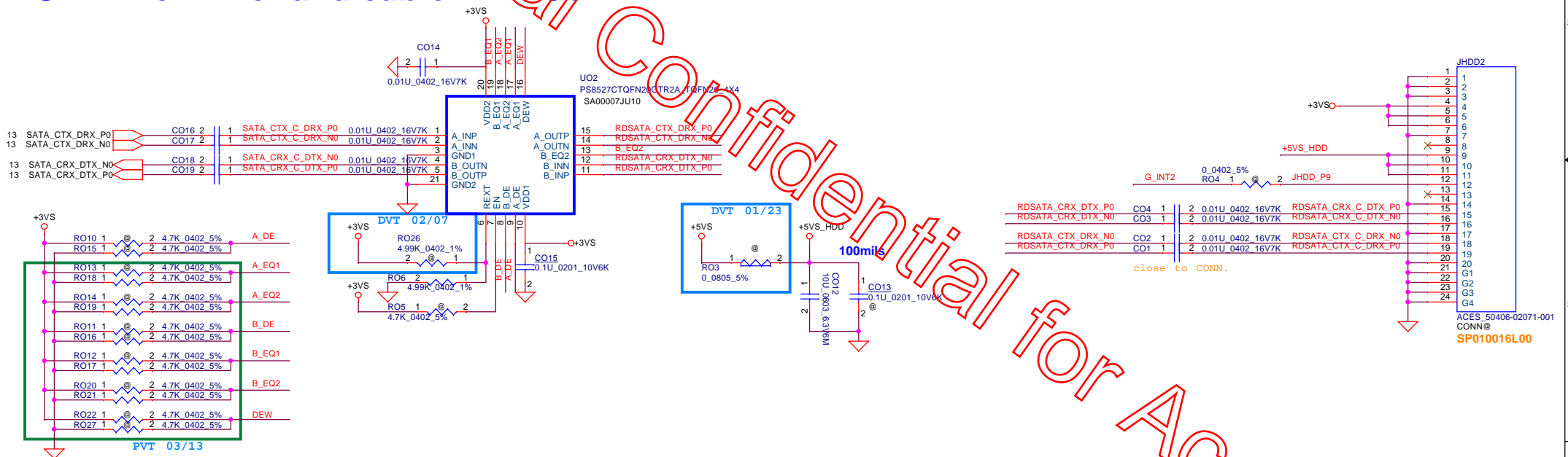


SATA ODD Conn.

(Reserved)



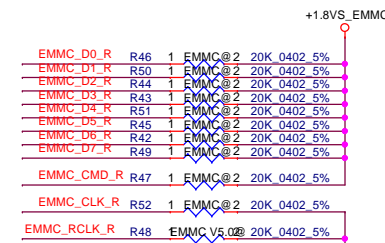
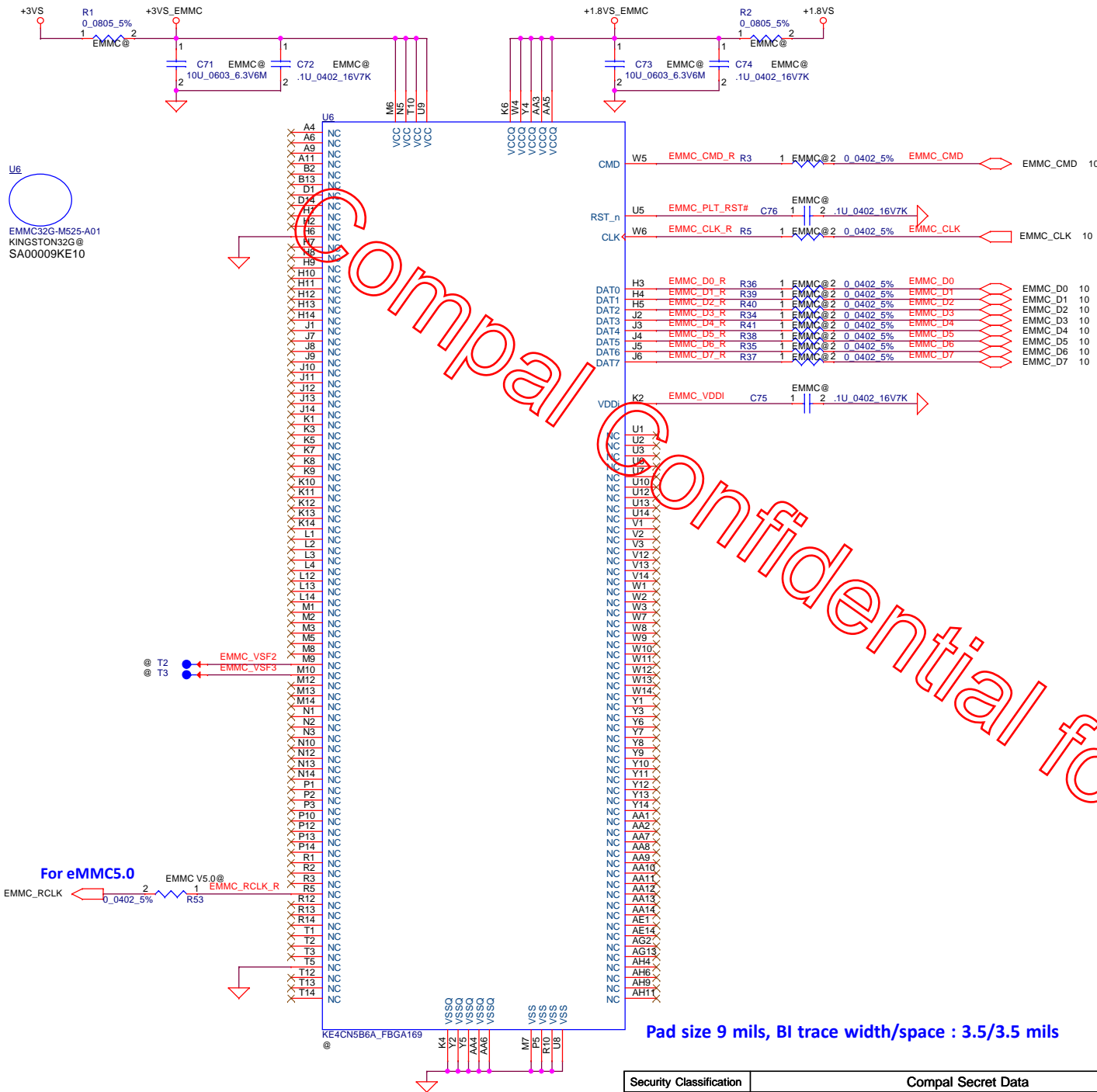
SATA Re-Driver and cable HDD Conn.



PS8527C EQ and DE

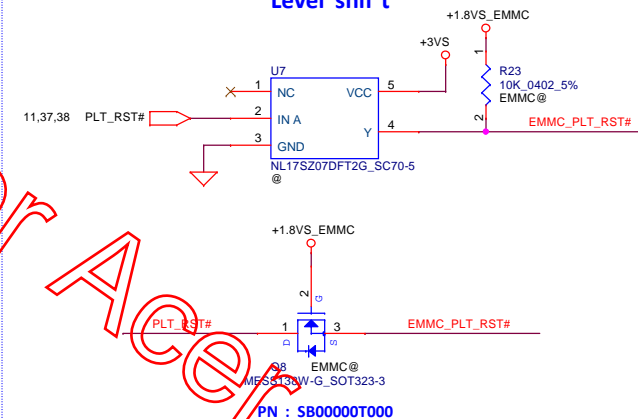
A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
* L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

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				Size	Document Number	Rev 1.A
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				Date:	Thursday, April 06, 2017	



Check if need pop for 5.0

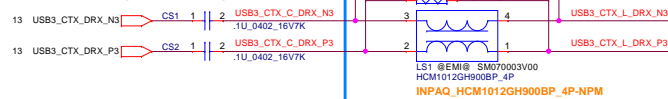
Level shift



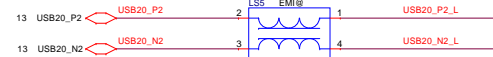
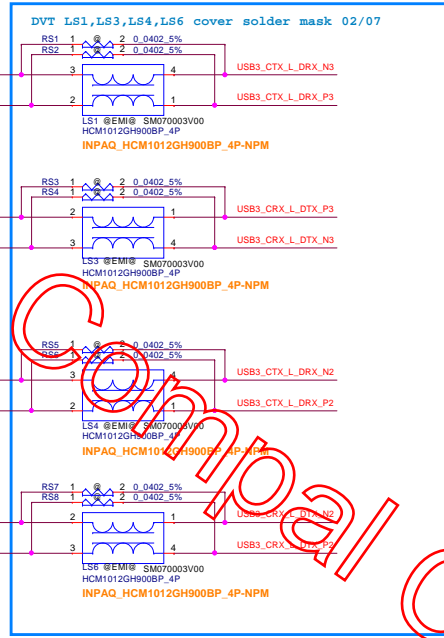
Pad size 9 mils, BI trace width/space : 3.5/3.5 mils

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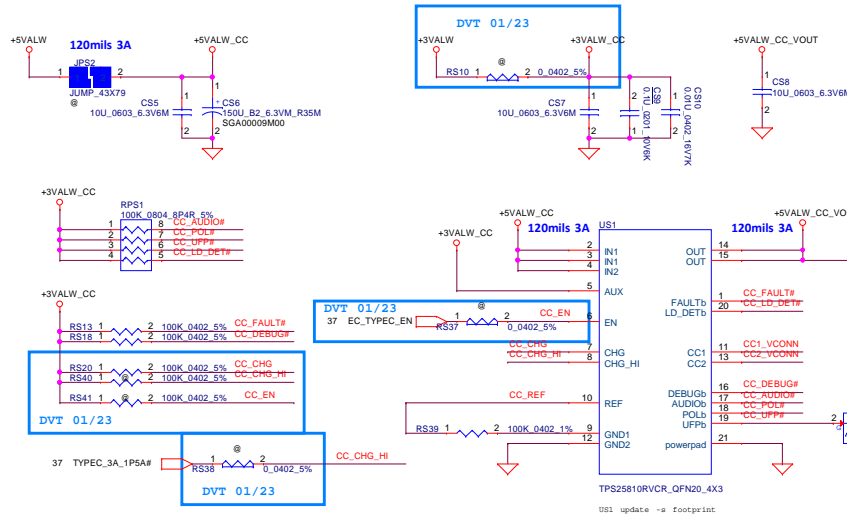
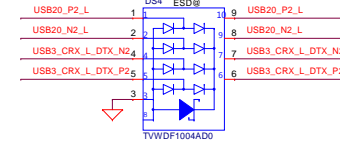
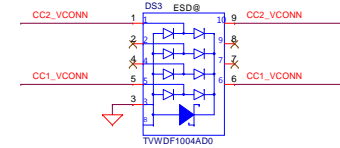
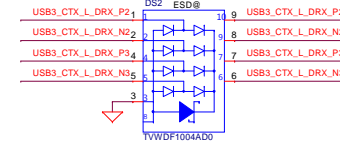
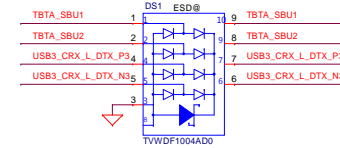
USB3.0 (Port 3)



USB3.0 (Port 4)



For ESD request



EC_TYPEC_EN	S0	S3	S5
AC Mode (Adapter In)	On	On	Off
DC Mode (Battery Only)	On	On ¹	Off

Note 1: Stop charge current when the battery capacity is below a specified percentage.
Note : 2017 BIOS SPEC define DC mode 30% stop charge

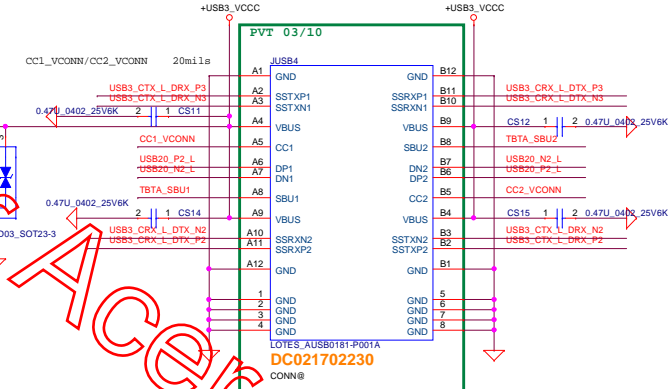
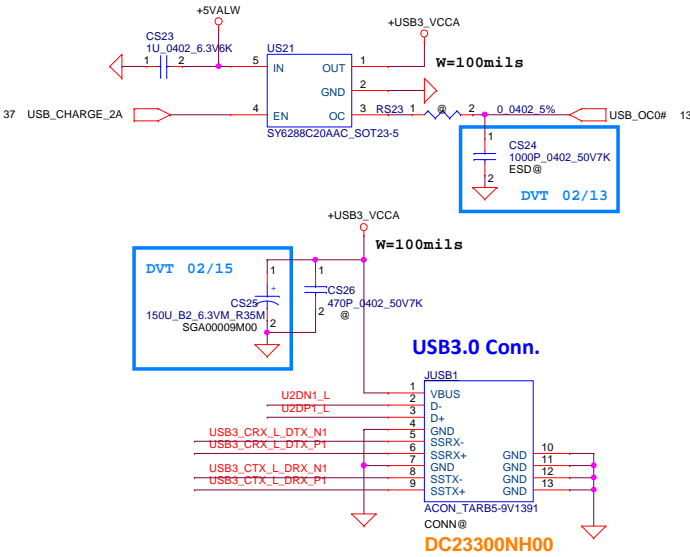
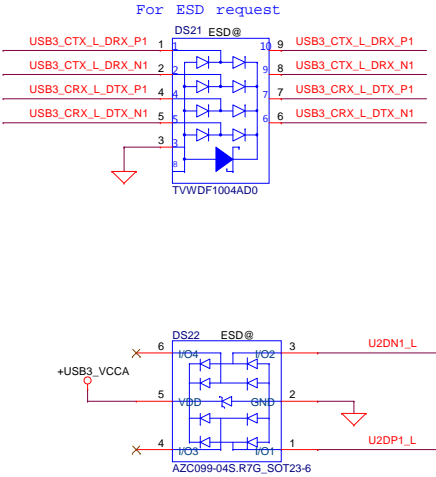
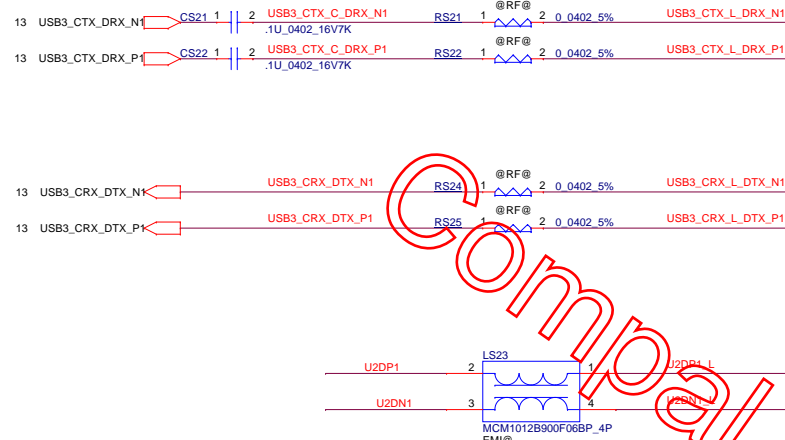


Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

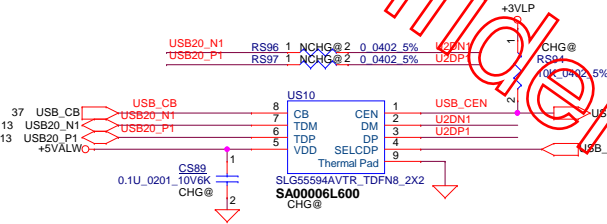
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USB3.0 (Port 1)

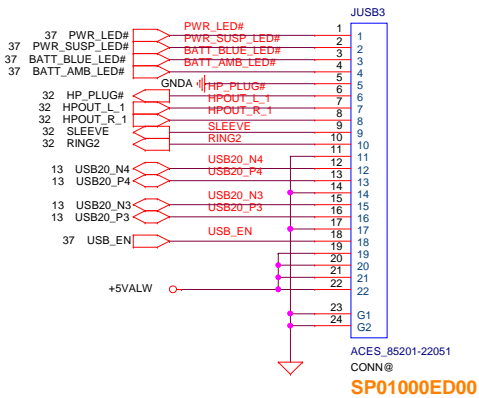


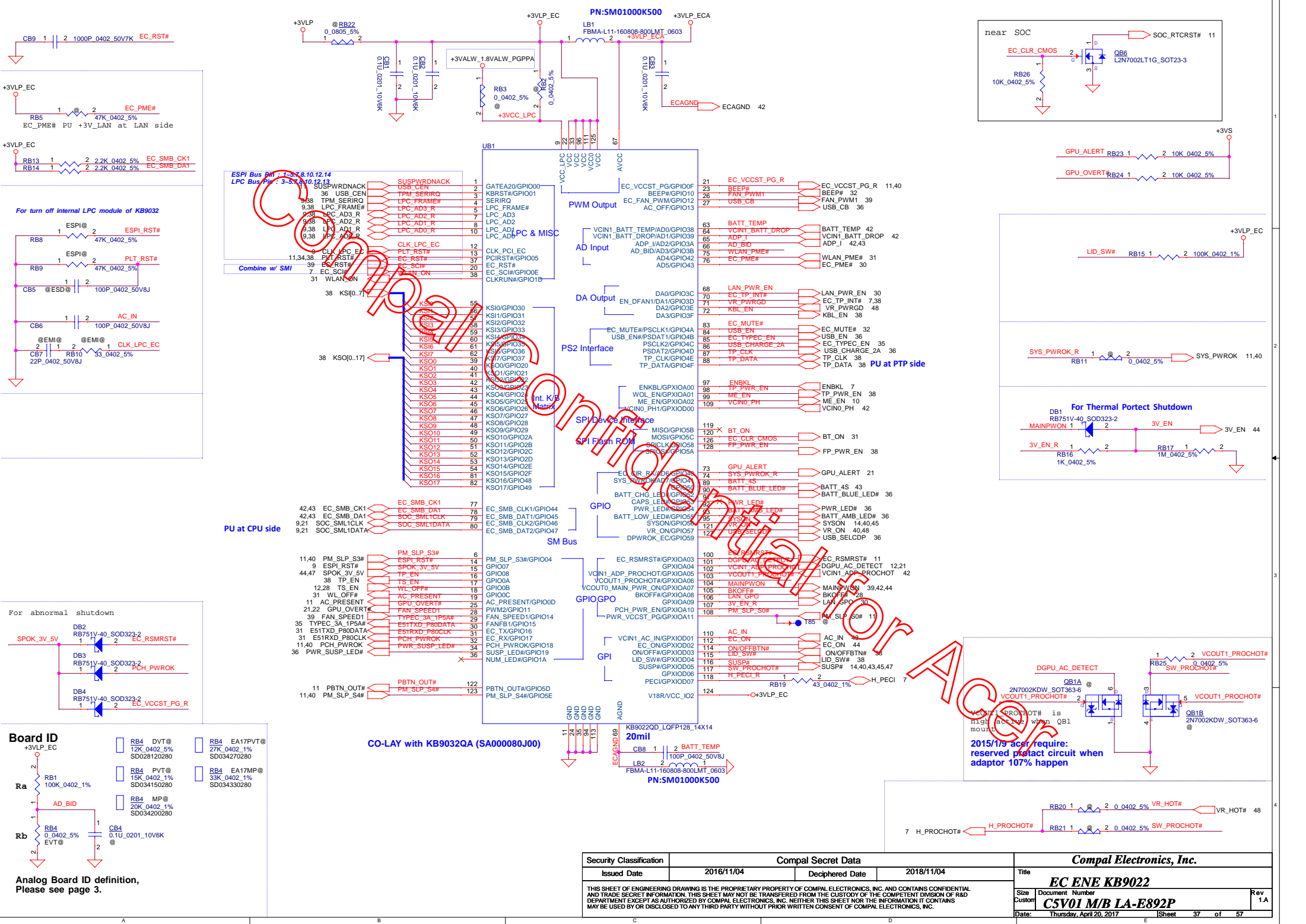
USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



USB/B (USBx2, AUDIO, LEDx2)

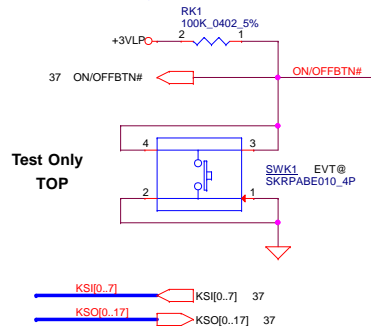




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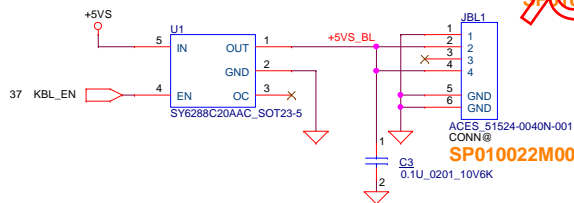
KB Conn.

ON/OFF BTN

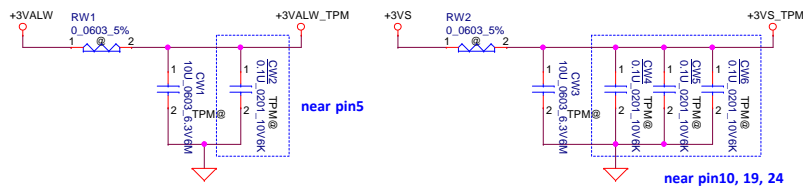


Test Only
TOP

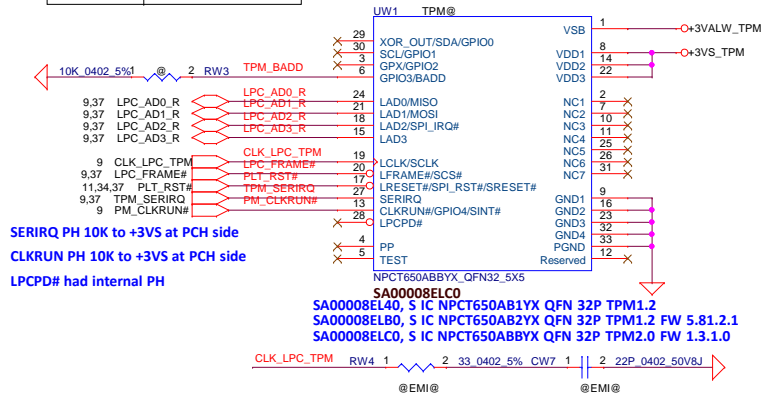
KB BackLight



TPM

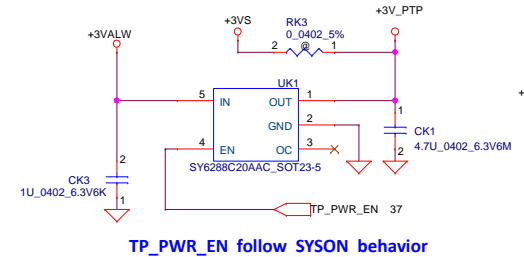


BADD	SELECTION
* 1	Aeh(write), Afh(read)

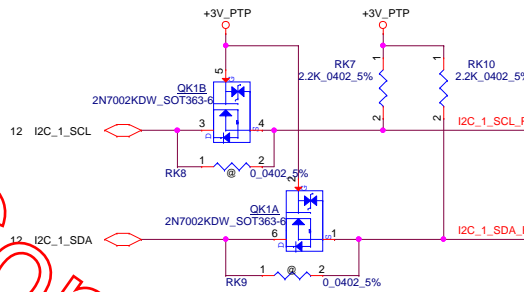


SA00008EL40, S IC NPCT650AB1YX QFN 32P TPM1.2
SA00008ELB0, S IC NPCT650AB2YX QFN 32P TPM1.2 FW 5.81.2.1
SA00008ELC0, S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0

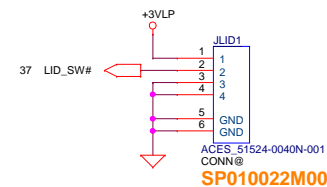
TP/B Conn.



TP_PWR_EN follow SYSON behavior

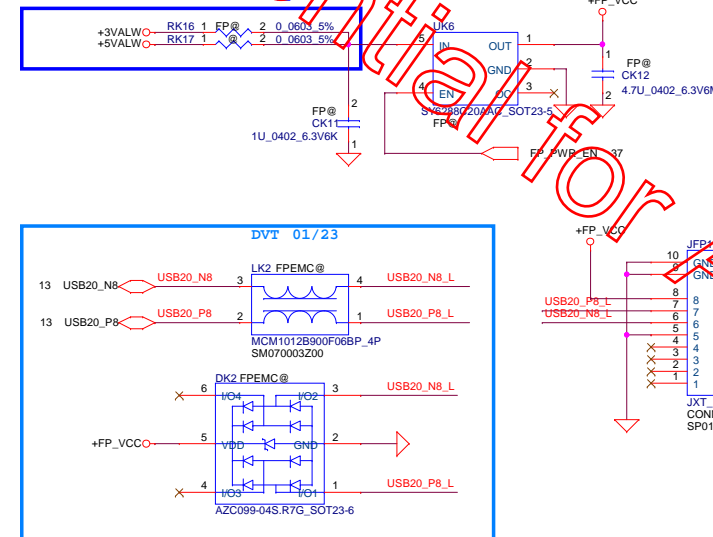


Lid Switch (Hall Effect Switch)



Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3V

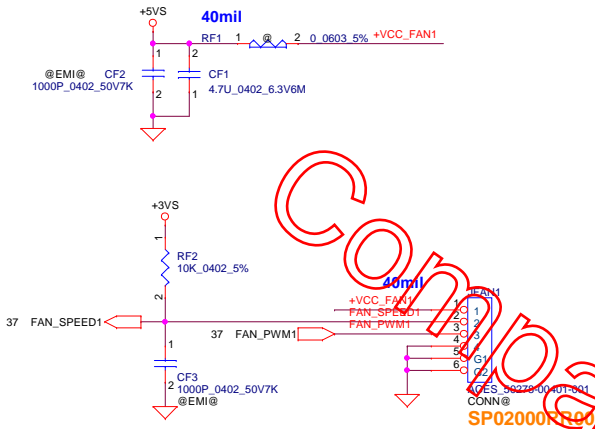


PIN	ETU801	SA464K-2200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
6	NC	NC
7	NC	NC
8	NC	NC

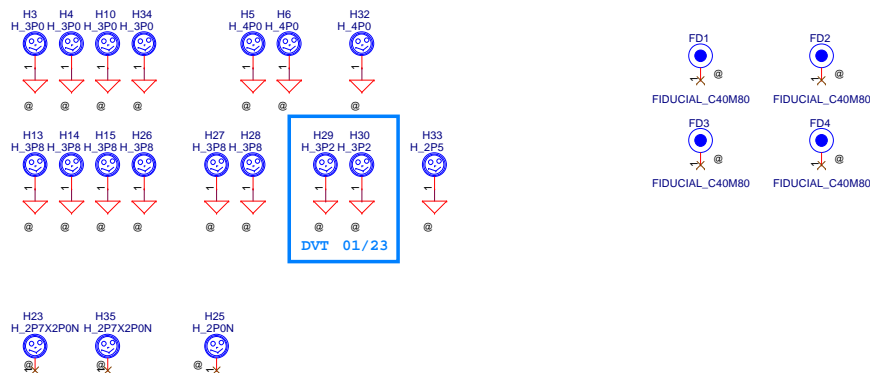
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Custom	C5V01 M/B LA-E892P	
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Rev	1.A	

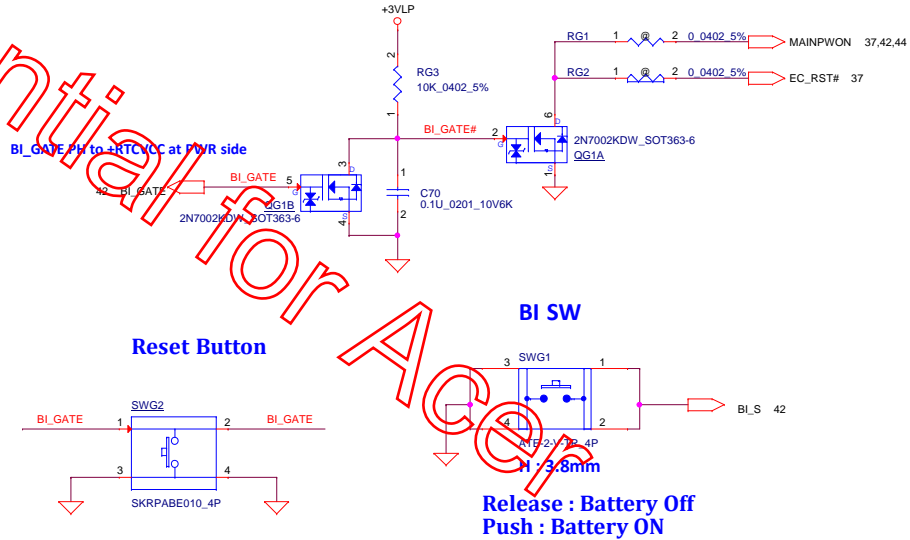
FAN1 Conn



Screw Hole

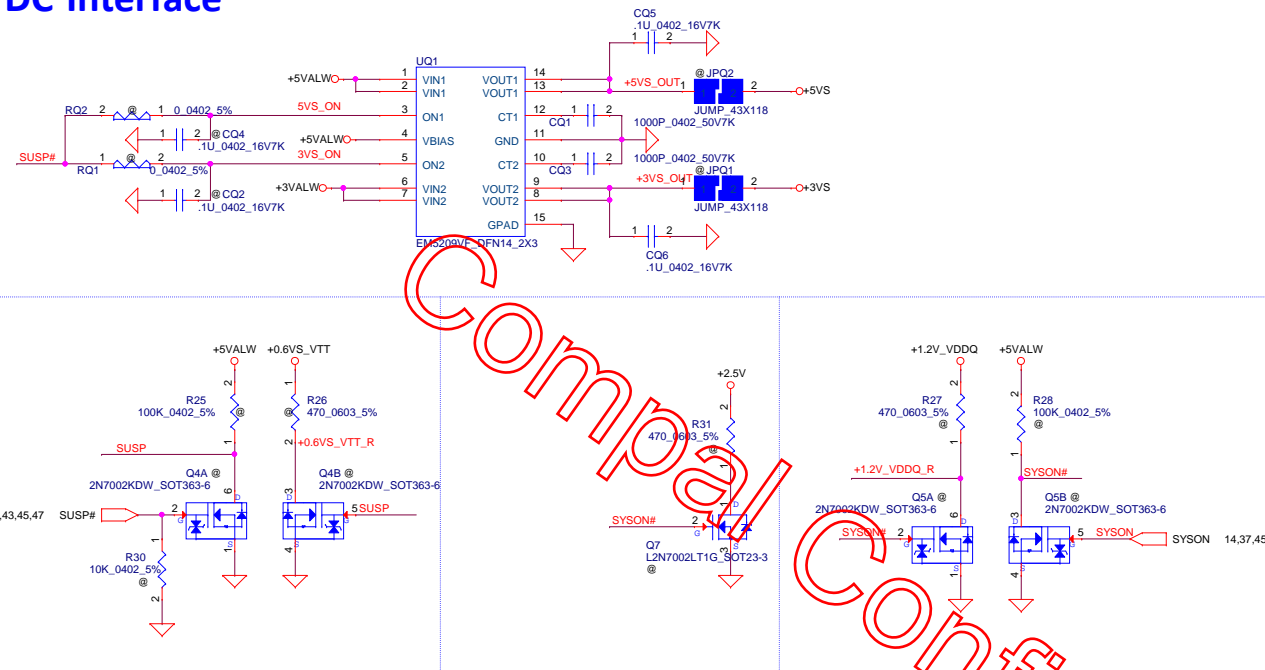


Reset Circuit

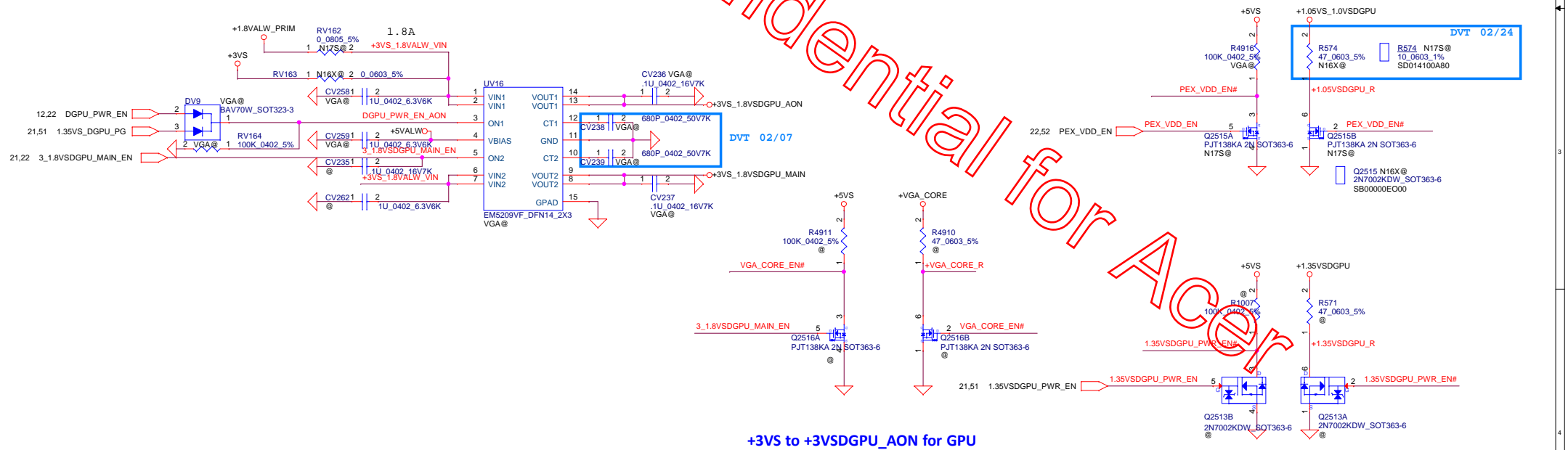
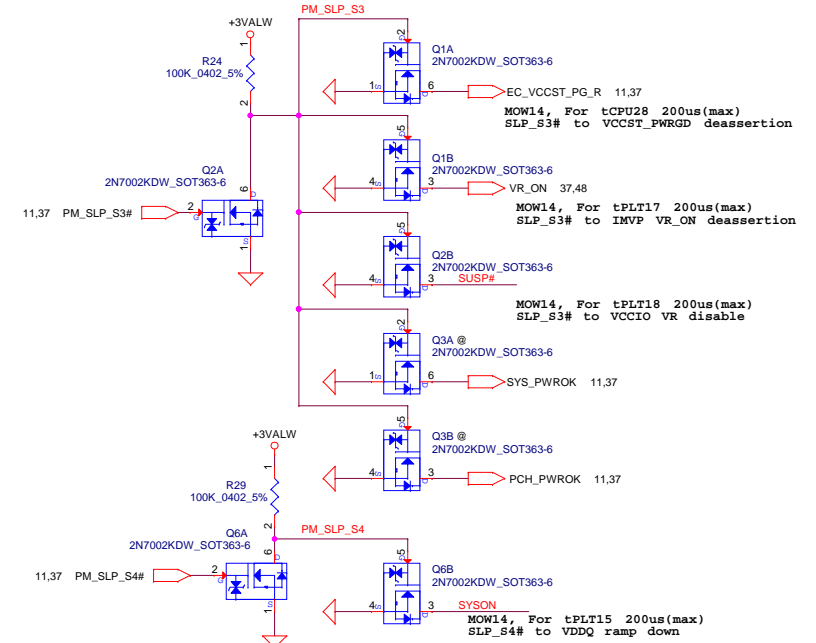


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Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title	FAN & Screw Hole & Reset
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				Customer	C5V01 M/B LA-E892P
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DC Interface

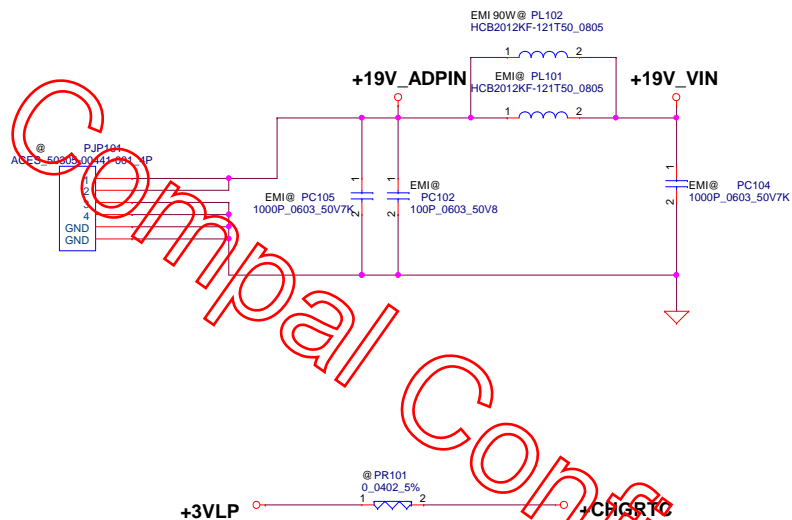


For Power ON/Off Sequence



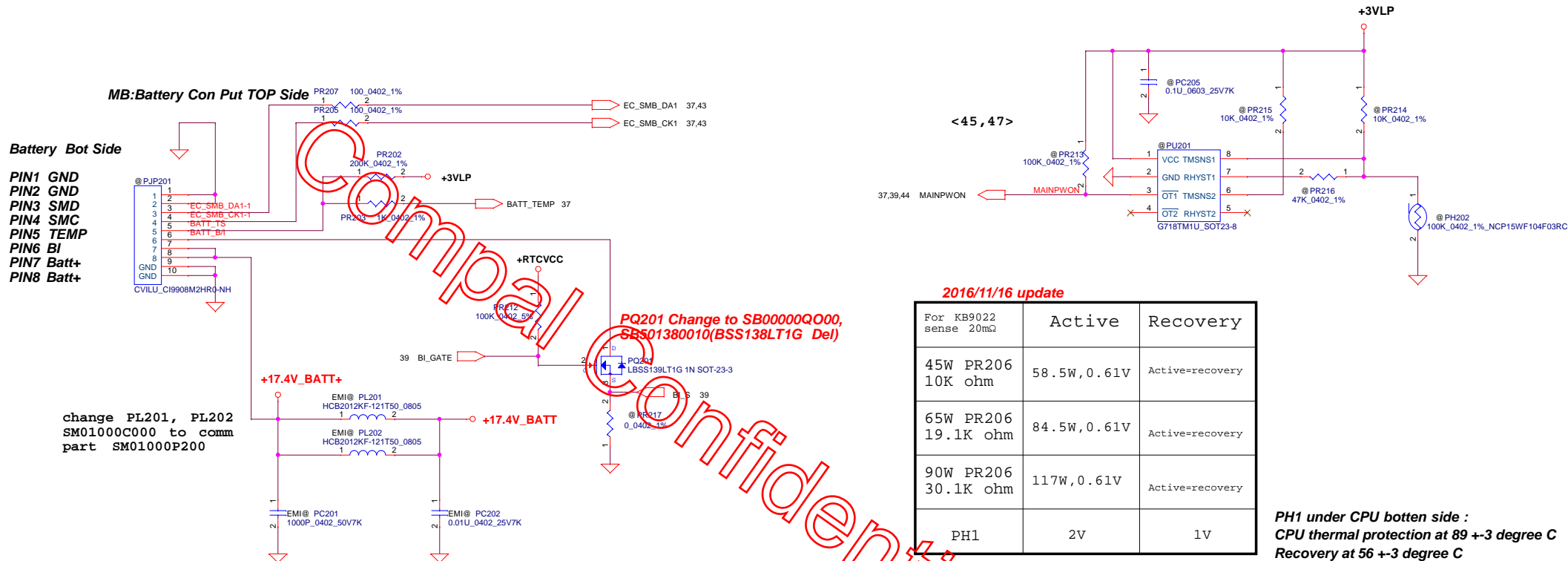
+3VS to +3VSDGPU_AON for GPU

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				Size	Document Number	Rev 1.A
				C5V01 M/B LA-E892P		
				Date:	Thursday, April 06, 2017	Sheet

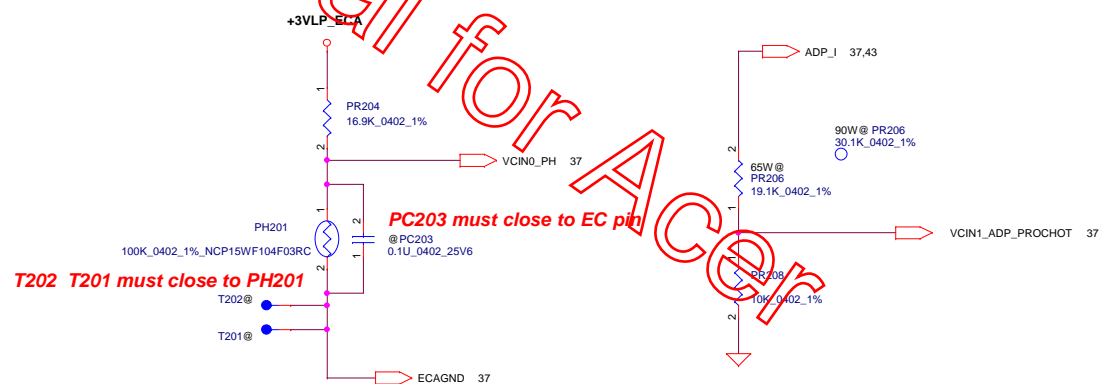
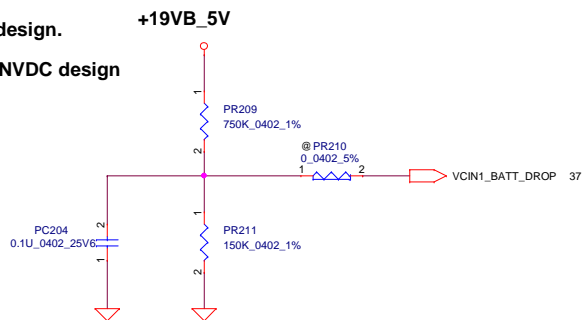


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Size	Document	Number	Rev	C5V01 M/B LA-E892P	
Custom	Date: Thursday, April 06, 2017			Sheet	41 of 57

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1



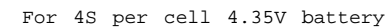
VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50K if Battery is 2-cell NVDC design
B+=6V



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Size		Document Number		Rev	
Custom		C5V01 M/B LA-E892P		0.1	
Date:		Thursday, April 06, 2017		Sheet 42 of 57	

Need check the SOA for inrush

$V_{gs} = 20V$
 $V_{ds} = 60V$
 $I_d = 250mA$


$$\begin{aligned} \text{VILIM} &= 20 \cdot \text{ILIM} \cdot \text{Rsr} \\ \text{ILIM} &= 3.3 \cdot 100 / (100 + 316) / 20 / 0.01 \\ &= 3.966 \text{ A} \end{aligned}$$

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	<i>Common Circuit</i>	0.1
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Module model information

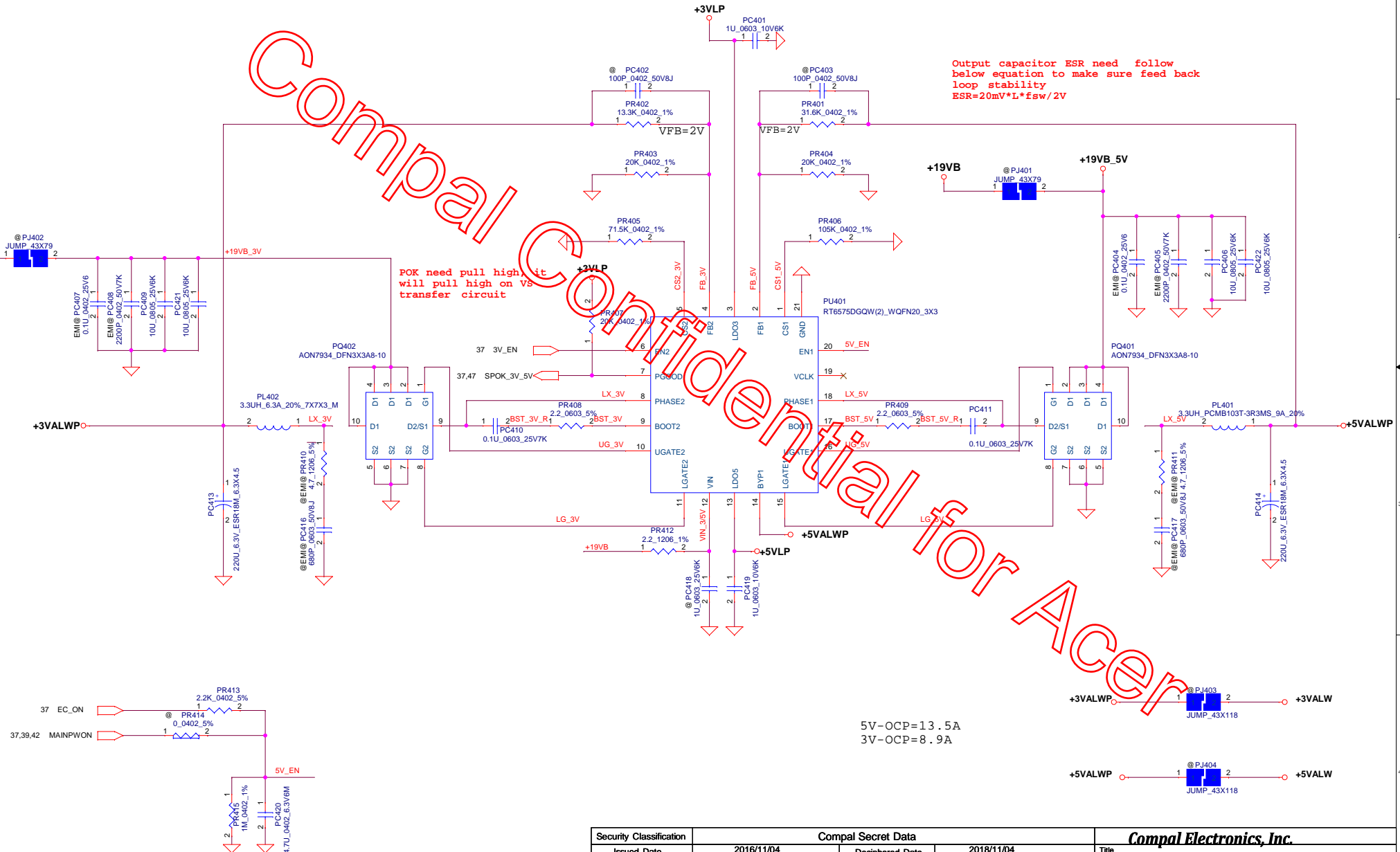
RT6575D_DMOS_single_V1.mdd
RT6575D_DMOS_dual_V1.mdd

H/S Rds(on):typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
Ploss=0.42W

L/S Rds(on):typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A, Idsm(TA=70)=9A
Ploss=0.14W

CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W

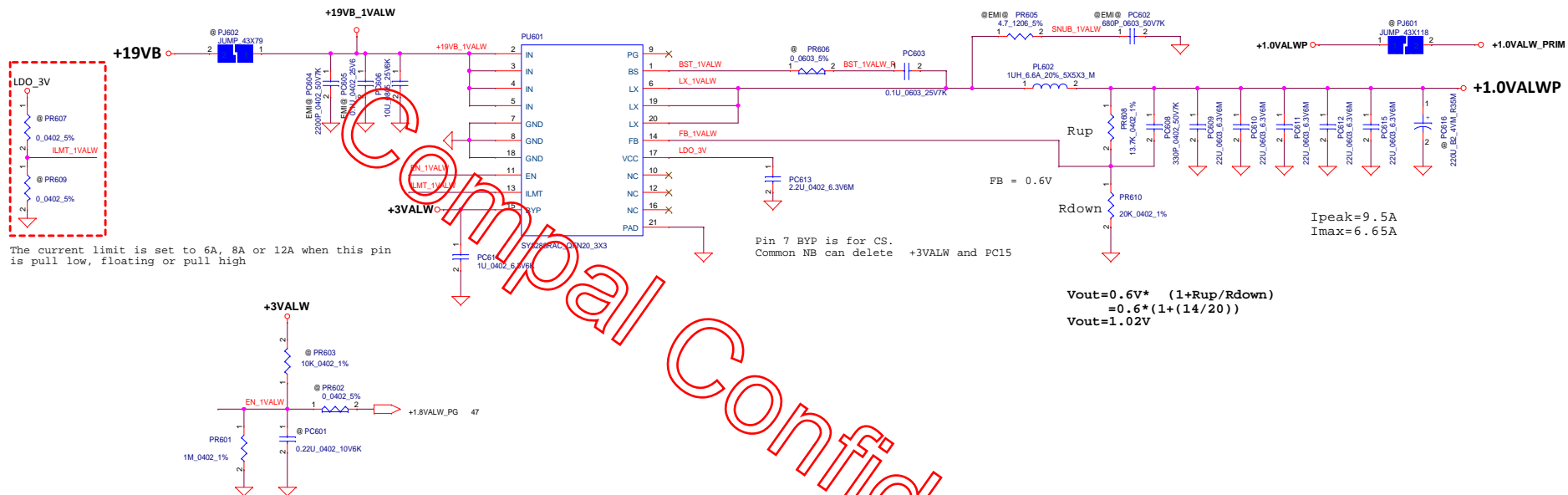
Output capacitor ESR need follow
below equation to make sure feed back
loop stability
 $ESR=20mV \cdot L \cdot f_{sw} / 2V$



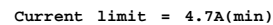
5V-OCP=13.5A
3V-OCP=8.9A

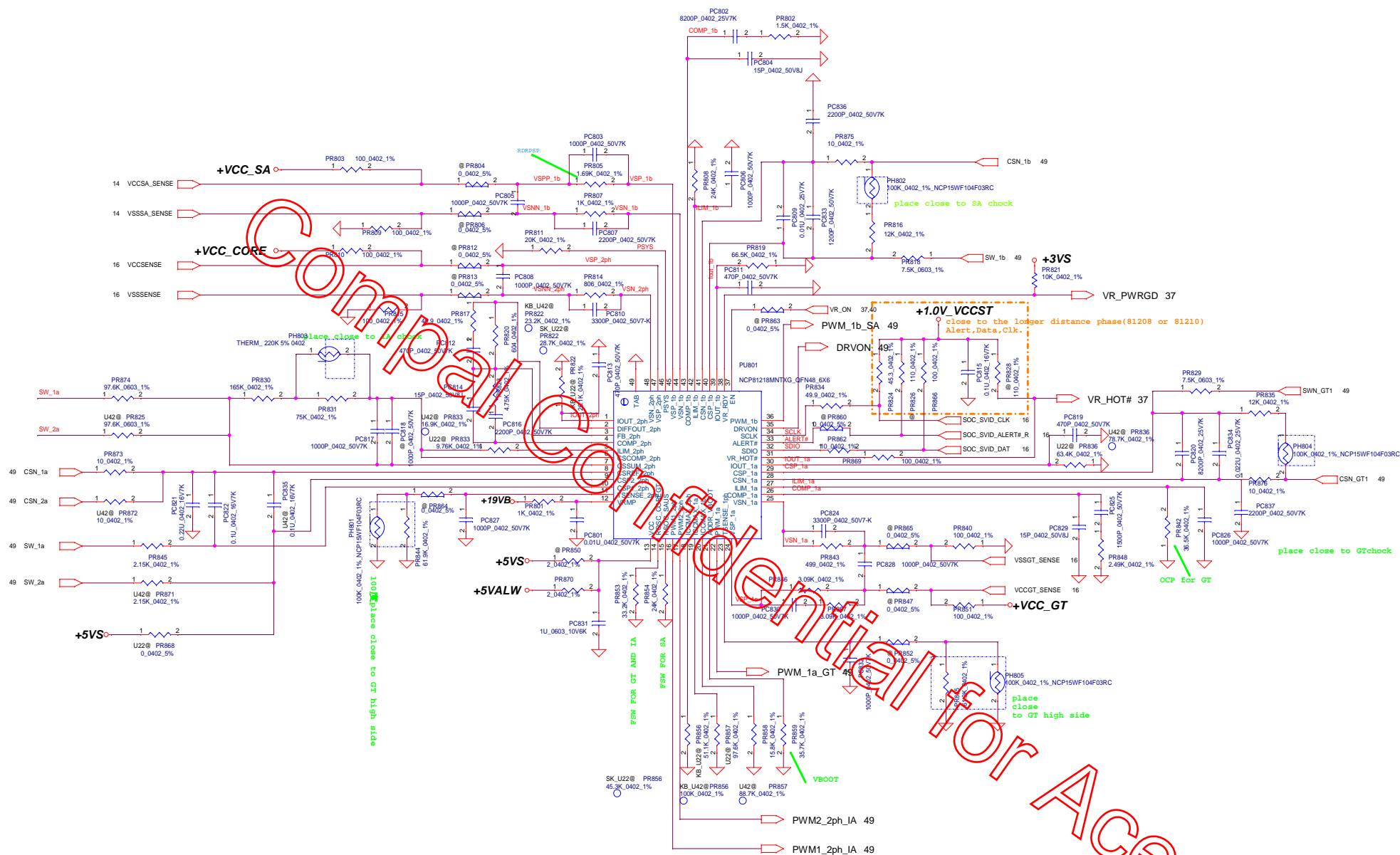
Security Classification		Compal Secret Data	
Issued Date	2016/11/04	Deciphered Date	2018/11/04
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Title		Compal Electronics, Inc.	
Size		PWR-3.3VALWP/5VALWP	
Document Number		CSV01 M/B LA-E892P	
Date		Thursday, April 06, 2017	
Rev		0.1	
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



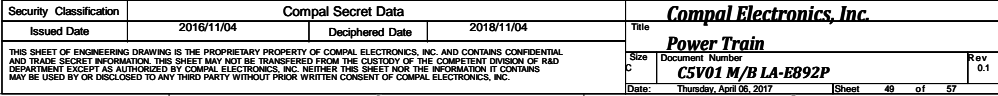
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>					
Issued Date		2016/11/04	Deciphered Date		2018/11/04	Title			
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						Size	Document Number		Rev
						C	CSV01 M/B LA-E892P		0.1
						Date:	Thursday, April 06, 2017	Sheet	46 of 57







A circuit diagram showing a blue Jumper component with two terminals labeled 1 and 2. Terminal 1 is connected to a red wire, and terminal 2 is connected to a red wire labeled +19VB. Above the jumper, the text "@ PJ901" and "JUMP 43X79" is displayed.



[illegible]

		GPU Core	GPU FBIO		FB Total ^{1, 5}		1.05V Total ²	3.3V Total
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴	3.3V ⁴
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5 @ 2.0 GHz	26.5	—	2.0	—	4.2	0.80	0.06
	GDDR5 @ 2.5 GHz	26.5	—	2.0	—	4.7	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GXR	GDDR5	35.4	—	2.4	—	4.9	2.6	0.40

		GPU Core	GPU FBIO		FB Total ¹⁻⁵		1.05V Total ²
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴
Products	VRAM Type	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	34.0	—	2.9	—	6.8	2.1
	DDR3/L	39.5	2.6	2.3	4.1	3.9	2.1
N16S-GTR	GDDR5 @ 2.0 GHz	53.0	—	2.9	—	6.8	2.1
	GDDR5 @ 2.5 GHz	53.0	—	3.1	—	7.2	2.1
	DDR3/L	51.0	2.6	2.3	4.1	3.9	2.1
N16S-GXR	GDDR5	54.0	—	4.6	—	9.5	2.9

	NVVD	GPU FBIO	FB Total ⁵	1.0V Total ¹	1.8V Total ²
	—	1.35V ⁴	1.35V ⁴	1.0V ⁴	1.8V ⁴
Product	(A)	(A)	(A)	(A)	(A)
N175-G1	29.7	2.0	3.4	0.1	0.3
N175-LG	15.4	1.6	2.8	0.1	0.2

	NVDD	GPU FBIO	FB TOTAL ⁴	1.0V Total ¹
	—	1.35V ³	1.35V ³	1.0V ³
Product	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2

Title		Compal Electronics, Inc.	
Size C		Document Number Power Train C5V01 M/B LA-E892P	
Date:	Thursday, April 06, 2017	Sheet	51 of 57
		Rev	0.1

Note:
 When design Vin=5V, please stuff snubber to prevent Vin damage

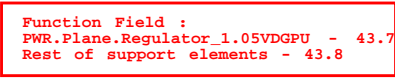
Function Field :
 PWR.Plane.Regulator_1.05VDDGPU
 Rest of support elements - 4

$$V_{out} = 0.6V * \left(1 + \frac{R_{up}}{R_{down}} \right)$$

$$\Rightarrow 0.6V * \left(1 + \frac{1.768 / 10}{6.81 / 10} \right) = 1.061 \quad (1.01\%)$$

$$\Rightarrow 0.6V * \left(1 + \frac{1.768 / 10}{6.81 / 10} \right) = 1.072 \quad (2.1\%)$$

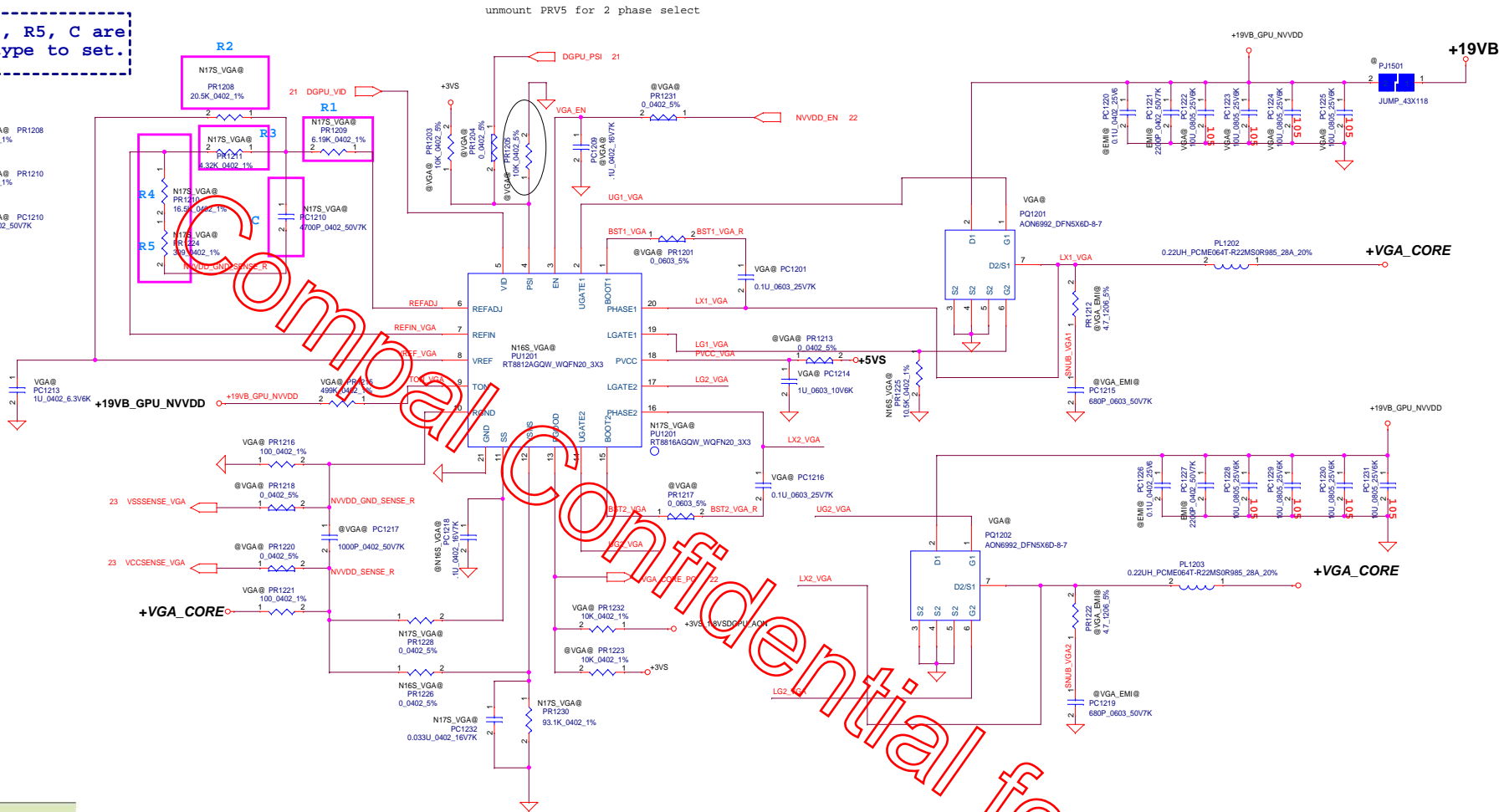
$$V_{out} = 0.6V * \left(1 + \frac{6.81 / 10}{1.768 / 10} \right) = 3.0086V$$


$$\begin{aligned} V_{out} &= 0.6V * (1 + R_{up} / R_{down}) \\ &= 0.6V * (1 + (7.68 / 10)) = 1.061 \quad (1.01\%) \\ &= 0.6V * (1 + (7.87 / 10)) = 1.072 \quad (2.1\%) \\ V_{out} &= 0.6V * (1 + (6.81 / 10)) = 1.0086V \end{aligned}$$

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R1, R2, R3, R4, R5, C are based on VGA type to set.

R1 N16S_VGA@ PR1209 20K_0402_1%
R2 N16S_VGA@ PR1208 20K_0402_1%
R3 N16S_VGA@ PR1211 2K_0402_1%
R4 N16S_VGA@ PR1210 10K_0402_1%
R5 N16S_VGA@ PR1224 0.0402_5%
C N16S_VGA@ PC1210 2700P_0402_50V7K



PWM-VID Specification		
		Config B
Vmin	V	0.6
Vmax	V	1.2
Vboot	V	0.9
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	96
PWM Frequency F _{PWM}	MHz	1.125
PWM Minimum Pulse Width T _{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	20
R2 (1%)	KΩ	20
R3 (1%)	KΩ	2
R4 (1%)	KΩ	18
R5 (1%)	KΩ	0
C	nF	2.7

N17x DG-07875-001_v08.pdf:

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25

Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification		
	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F _{PWM}	kHz	675
PWM Minimum Pulse Width T _{DMIN}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.309
C	nF	4.7

Table 6. EDP-Continuous³

Products	VRAM Type	GPU Core
N16S-GMR	GDDR5	19.0
	DDR3/L	21.0
N16S-GTR	GDDR5 @ 2.0 GHz	26.5
	GDDR5 @ 2.5 GHz	26.5
	DDR3/L	26.0
N16S-GXR	GDDR5	35.4

Table 7. EDP-Peak³

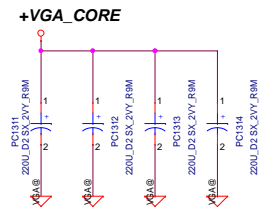
Products	VRAM Type	GPU Core
N16S-GMR	GDDR5	34.0
	DDR3/L	39.5
N16S-GTR	GDDR5 @ 2.0 GHz	53.0
	GDDR5 @ 2.5 GHz	53.0
	DDR3/L	51.0
N16S-GXR	GDDR5	54.0

Table 7. Output EDP-Continuous

	NVVD	GPU FBIO	FB Total ⁵	1.0V Total ¹	1.8V Total ²
Products	(A)	(A)	(A)	(A)	(A)
N17S-G	29.7	2.0	3.4	0.1	0.3
N17S-LG	15.3	1.9	2.8	0.1	0.2

Table 8. Output EDP-Peak

	NVVD	GPU FBIO	FB TOTAL ⁴	1.0V Total ¹
Product	(A)	(A)	(A)	(A)
N17S-G1	59.2	3.2	6.6	0.2
N17S-LG	49.6	3.2	6.6	0.2



Version change list (P.I.R. List)

Page 1 of 1
for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	prevent part damage				PC410 and PC411 change to 0603 size	1/23	DVT
02	reduce part count				PR515,PR804,PR806,PR812,PR813,PR865,PR847,PR860,PR876,PR863,PR852,PR864,PR875,PR901,PR912,PR904,PR913,PR914 change to R-short	1/23	DVT
03	voltage level too high	3.37V change to 3.33V			PR402 change to 13.3K from 13.7K	1/23	DVT
04	SPOK voltage level				PR407 change to 20K from 100K	1/23	DVT
05	SMT	close SMT stencil problem			PJ9001, PJ9002, PJ9003 change to 0.2m ohm	1/23	DVT
06	DC S5 power consumption	meet DC S5 2.5mA spec			PR209 change to 750K from 10K PR211 change to 150K from 2K	1/23	DVT
07	prevent shortage				PL907 change to common part SH00001ED00 PQ502 change to AON7506	1/23	DVT
08	For N17s colay N16S				add PR1015 Oohm and PC1018 for transient PR1009 change to Oohm from R-Short PR1013 change to Oohm from 100 ohm	1/23	DVT
09	For power sequence				PC1218 change to unpop for rise time PR1231 change to 1K from 20K for sequence PR1003 change to 100K from 1M PR1002 change to Oohm from 40.2K	1/23	DVT
10	For EMI request				PJ301 change to PL301	1/23	DVT
11	CPU transient	meet CPU spec			PR805 change to 1.69K from 1.78K PR814 change to 806ohm from 1K PR874 change to 97.6k from 93.1K PC821 change to 0.22u from 0.1uF PC820 change to 8200P from 0.01uF PR836 change to 63.4K from 69.8K PR846 and PR867 change to 3.09K from 3.32K PC9002,PC9003,PC9099,PC9098,PC9014,PC9091,PC9048 change to dummy	2/8	
12		1. prevent N17S design change 2. 5V voltage change to 5.2V 3. HW request 4. add filter 5. for mode change			1. PR701,PR1204,PR718,PR1201,PR1217 change to Oohm from R-short 2. PR401 change to 31.6k from 30.9K 3. add PR1232 for VGA CORE PG and PU to +3VS_1.8VSDGPU_AON. 4. PR1223 change to un-pop PC836 and PC837 change to pop PR875 and PR876 change to 10ohm PR908 change to 0 ohm 5. PU901 and PU902 change to NCP81151MNTBG_DFN8_2X2 PU903 change to NCP81253MNTBG_DFN8_2X2	2/9	
13		power squence			PC1209 change to unpop PR1231 change to R-short	2/10	
14		5V OCP level change			PR406 change 105K from 107K	2/19	
15		VGA Voltage overshoot reduce part count VRAM fix 1.35V			add PC1232 0.033uF PR718,PR1015,PR1013,PR1101,PR1204,PR1201,PR1217,PR1002change to R-short PR1010,PQ1001,PR1009,PR1011 remove from BOM	3/15	
16		component rating Add RC delay			PC1215 and PC1219 size change to 0603 from 0402 PR320 change to 499 ohm PC323 change to pop 2.2uF	3/24	

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Size	Document	Number	Rev	
Custom	B5W1S M/B LA-D671P		0.2	
Date:	Thursday, April 06, 2017	Sheet	55	of 57

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
1	35	1/23	1.0	Type-C change connector	JUSB4 Symbol change to LOTES_AUSB0249-P001A_24P-T
2	38	1/23	1.0	Modify BOM structure	LK2, DK2 Change to FPENC@
3	39	1/23	1.0	ME Drawing update	H30,H29 Change to H_3P2
4	30	1/23	1.0	Update for SD Card write protect issue	Add QL1 & RL20, RL21, RL22 for SD_WP inverter circuit
5	31,33,35	1/23	1.0	Change 0 ohm to R-Short	RM9,RO3,RS10,RM23,RS37,RS38 Change to R-short
6	19	1/23	1.0	For acer lesson learnt V1.7	RD202 Change to 0 ohm (DDR_DRAMRST#)
	11				Reserve CC131 on EC_VCCST_PG
	11				Add RC20 10_0402_5% ohm (PCH_PWROK)
	15				POP CC123 AND Change to 10U_0603
7	36	1/23	1.0	Cap. package Change	CS24 Change to 0402 package
8	33	1/23	1.0	Remove un-use connector	Del JHDD1
9	31	1/23	1.0	Follow ESD request	POP CM15 with 1000pf
10	22	1/23	1.0	Update VGA Power Sequence(+1.05VS_1.0VSDGPU)	Unpop RV103, CV231 Add RV188 from VGA_CORE_PG
11	32	1/23	1.0	EMI Requirement change to 220ohm bead	Change RA34 to SM01000NY00(BLM15PX221SN1D) with EMI@
12	22	2/7	1.0	Add N17S Component for BOM Select	Add UGPU1 SA0000ANV00 with N17SG1@ Change BOM structure from GTR@ to N16SGTR@ Del UGPU1 for GMR1@ Add X7607@,X7608@,X7609@
13	12,35	2/7	1.0	Change 0 ohm to R-Short	RC195, RC204, RS1,RS2,RS3,RS4,RS5,RS6,RS7,RS8 change to R-Short
14	33	2/7	1.0	Adjust SATA TX redirver EQ for Parada IC	RO17, RO18 and RO19 change to X76PAR@
15	33	2/7	1.0	Update SATA redriver circuit for TI IC	Reserved RO26, RO27 with BOM strurture @ Add RO17, RO18 (4.7K), RO19, RO21 (0 ohm) with X76TI@
16	29,22	2/7	1.0	BOM Change	Pop CC58 with 10uF, unpop CC59
17	40	2/7	1.0	Update VGA Power Sequence	CV238, CV239 change to 680PF
18	8	2/7	1.0	Add CPU PN for DVT	Add UC1 PN for Intel i3,i5,i7 CPU
19	13,35	2/7	1.0	Remove un-use USB port(Port9)	Del LS24
20	35	2/7	1.0	Bom Change , pull up resistor change to 100K ohm	RS20, RS40,RS41 value change to 100k ohm
21	36	2/7	1.0	Cancel solder mask on co-lay pin	LS1,LS3,LS4,LS6 cover solder mask (footprint update)
22	36	2/8	1.0	For acer lesson learnt V1.7	CC65.1 change to PCH_PWROK_R
23	18	2/8	1.0	Adjust Crystal Cap value	CC128,CC129 change to 27pF
24	8	2/8	1.0	Update PCB PN	Add DAZ20X00201 and DA8001AU010 for PCB
25	32	2/8	1.0	Update BOM Structure	Change RA35 BOM Structure to EMI@
26	22	2/10	1.0	For N17S GC6 Discharge Sequence	Add DV10 Add RV189, CV263, DV11
27	9	2/10	1.0	Remove BIOM ROM socket (Debug only)	Del JC1
28	7,11,36	2/13	1.0	For acer lesson learnt V1.7	Add CC132 Change to 1000pF --> CC50, CC53,CC131,CS24,CC65
29	36	2/13	1.0	Change Cap material for Z-High issue	Change CS25 to SGA00009M00
30	21,30	2/15	1.0	Change R for 25M/27M Crystal	Change R4961 and RL14 to 1K
31	21	2/16	1.0	Change 27MHz Material	X2000 change from SJ10000UI00 to SJ10000TQ00
32	18	2/16	1.0	Connect UC1.F65/G65 to GND, Change AY3, AY71 NC	Add RC237, Change RC182,RC183 to 0 ohm(@)

HW Schematic chang list (P.I.R)

[illegible]

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